OPTOFLUIDIC MANIPULATION AND PACKAGING OF SILICON MICROCHIPS USING RAINED MICROFLUIDICS

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ABSTRACT
We demonstrate fluidic manipulation and assembly of silicon microchips by creatively combining railed microfluidics and computer-vision aided dynamic chip packaging. Externally fabricated silicon microchips are fluidically guided and self-assembled, potentially enabling low cost fluidic packaging of integrated circuits.

KEYWORDS: Railed microfluidics, Optofluidic maskless lithography

INTRODUCTION
In the integrated circuit industry, the cost effective packaging of small chips are of utmost importance. The chip size of radio frequency identification (RFID) and light emitting devices (LED) currently in commercial production are smaller than 200 µm. Conventional serial pick and place in this small scale suffers from high costs and low throughput, and fluidic self-assembly is demonstrated to be a great alternative [1]. Recently, we have demonstrated railed microfluidics as an agile method to guide and assemble in-situ photopolymerized microstructures inside fluidic channels [2]. This paper describes its applicability in industrial processes such as integrated chip packaging by fluidically controlling externally fabricated silicon chips.

THEORY AND EXPERIMENTAL RESULTS
Silicon microchips are fabricated externally (Fig.1). These chips can be thought of as a conceptual substitute for CMOS devices or LEDs.

Figure 1. Fabrication process of Si microchips (100 µm x 100 µm) (a) 100µm sized microchips patterning as an etch mask on a cleaned SOI wafer. (b) Deep reactive ion etch through 20µm device layer and remove photoresist. (c) Release Si chips using HF solution, filter with filter paper, and cleaning with D.I. water (d) Collect diluted silicon chips in D.I. water.
Figure 2. (a) Polymer packaging and fin generation process of a silicon microchip. (b) 1) Externally fabricated silicon microchips are introduced in microfluidic channels, 2) UV patterning of polymer package around silicon microchips, SEM image, 3) UV patterning of guiding fin structure on top of the polymer package, SEM image, 4) Silicon microchip with polymer package and fin structure is guided and assembled at the end of the rail

For fabrication of ‘fin’ structure necessary for rail-guiding of chips in fluidic channels, we packaged them with polymer via optofluidic maskless lithography system [3]. Fig. 2 shows polymer packaging and fin generation process. First, externally fabricated silicon particles mixed with oligomer solution are introduced into a channel (①). A rectangular UV mask pattern slightly bigger than the silicon chip is exposed to the chip (②). When the packaged chip reaches the rail layer, fin structures for the guide are generated on top of the polymer package (③). Therefore, silicon chips in the polymer package can be guided and assembled using the rail (④).

Figure 3. Image processing for rotational alignment of Si chips and uniform thickness of polymer packaging (a) CCD bitmap image of Si chips (b) Image conversion in MATLAB (c) DMD mask generation via image processing in MATLAB (d) UV patterning via OFML. Inset shows corresponding fluorescent microscopic image

In order to consider rotational alignment and orientation of silicon chips during polymer packaging or fin generation process, we used image processing of silicon chip image acquired by CCD and dynamically generated corresponding mask pattern
on DMD (Fig. 3(a)-(d)). Owing to the computer vision and imaging processing based optofluidic maskless lithography, uniform thickness of polymeric packaging of silicon chips are easily achieved.

Externally fabricated chips can be guided and assembled using the rail. Fig. 3 (a) shows railing silicon microchip with polymer package and fin structures. This silicon chip can be guided along the rail as shown in Fig. 3(b). We also fluidically placed multiple silicon chips with equidistance due to the uniform thickness polymer package (Fig. 4 (c)). Placing chips with equidistance has commercial implications for LED-based back-light unit or LED lighting packaging where a large number of small LED chips need to be placed in a larger substrate, such as a glass plate or a silicon wafer.

![Figure 4. Simple manipulation and assembly of packaged Si microchips (a)-(b) Time sequential images of guided movement of the silicon chip using the rail. (c) Assembly of chips on the rail. We fluidically placed multiple silicon chips with desired spacing by adding spacers in the polymer package.](image)

**CONCLUSIONS**

The fluidic control method of devices in railed microfluidic channel has been demonstrated as an innovative technique to manipulate microscale silicon chips. With polymer packaging and fin generation, we manipulate silicon chips effectively in a channel. We envision that uniform polymer packaging layer control will be useful for integrated CMOS chip or LED packaging.

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**REFERENCES**

