ROBUST LAYOUT TECHNIQUES DECREASE VOLUME INJECTION AND CAPACITIVE MISMATCH DUE TO ALIGNMENT ERRORS

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ABSTRACT

As functionality of pressure driven microfluidics increase, structural complexity will also increase. Future devices will not only require accurate flow resistance but will also depend on accurate component capacitances. Using the microfluidic serial DAC (digital to analog converter) as an example, we propose and demonstrate two robust layout techniques for designing multilayer microfluidic devices. The result of incorporating these design strategies is a more linear transfer function that does not depend on the diameter of capacitive membranes of the microfluidic serial DAC.

KEYWORDS: PDMS Microfluidics, Microfluidic Serial DAC, Robust Layout Strategy

INTRODUCTION

As the complexity of PDMS (Polydimethylsiloxane) microfluidic chips and on-chip control structures increase, accurate functionality requires tighter tolerances on the geometry of chip components. Even though most pressure driven multilayer microfluidic devices today are not critically dependent on the capacitance of their components, it is conceivable that proper functionality of future devices will depend on these capacitances. Analogous to the electronic manufacturing, tighter tolerances on component properties require more accurate fabrication processes. However, unlike the electronic industry, current PDMS molding techniques are still subjected to significant alignment errors between different PDMS layers. In order to maintain desired capacitive characteristics for microfluidic chips, we describe in this work two design strategies that is insensitive to small alignment offsets.

As an example microfluidic device that depends on its capacitive characteristics, we use the microfluidic serial pressure digital to analog converter (DAC). The functionality of this microfluidic device was previously demonstrated [1]. In addition to basic functionality, we also characterized its output linearity and concluded that output nonlinearity is mostly derived from capacitive mismatch and volume injection [2]. In this work, we propose two design methods to reduce effects of volume injection and capacitive mismatch due to fabrication related errors. Even though we will be exclusively referring to how these techniques improve output linearity of the microfluidic DAC, the same techniques are applicable to a broad class of capacitance dependent microfluidic chips as well [3].

THEORY

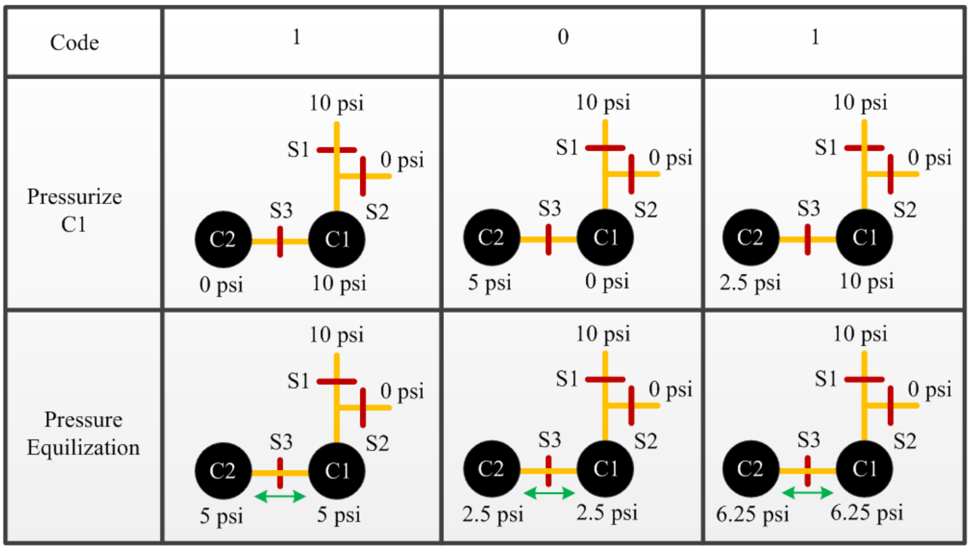

Figure 1: Microfluidic serial pressure DAC functionality depends on two operations per cycle. During each cycle, C1 is pressurized to 10 psi or 0 psi depending on the digital code. Then, switch S3 is used to perform pressure equalization, where pressures in C1 and C2 are set equal. This figure demonstrates steps required to generate 6.25 psi with a 10 psi supply and a 3 bit digital code of 5 (or 101 in binary). The code is processed from the most significant bit to the least significant bit.

Fig. 1 serves as a brief introduction to the functionality of the microfluidic serial DAC. This device is composed of two layers, the bottom layer includes control channels outline in red. These control channels are push up valves that depress flow channels above them. The second layer consists of flow channels in yellow and cylindrical chambers in black. Covering the cylindrical PDMS chambers are diaphragms acting as microfluidic capacitors. The microfluidic serial DAC functions based on pressure equalization. With a constant Pmax, the device could generate analog pressure levels between 0 and Pmax. During each actuation cycle, C1 is pressurized to Pmax or depressurized to 0. Then, pressure equalization is performed with S3. If C1 and C2 are the same, pressure on C2 after each actuation cycle moves half way closer to 0 or half way closer to Pmax (Eqn. 1). This property creates a simple way of generating an arbitrary pressure on C2 using a sequence of actuation cycles, each representing a bit in the binary representation system. More specifically, to create a pressure equivalent to 5/8 * Pmax on C2, a 3 bit code 101 is used (Fig. 1).

$$P_{C2}(n+1) = \frac{P_{C2}(n)}{2} \quad if \quad P_{C1}(n) = 0 \quad or \quad P_{C2}(n+1) = \frac{1 - P_{C2(n)}}{2} + P_{C2}(n) \quad if \quad P_{C2}(n) = 1 \qquad (1)$$

Ideally, output of the DAC should be linear and insensitive to actual sizes and thicknesses of PDMS capacitive membranes. In reality, transfer function of the serial DAC was not linear due to different amount of channels connected to C1 and C2 in Fig. 1. These channels introduce different channel capacitances to C1 and C2, accentuating capacitive mismatch. According to simulation, mismatch between these two capacitors will create nonlinear transfer functions. (Fig. 2b). Even if we use dummy channels to match the desired channels lengths attached to C1 and C2, alignment errors often still occur during bonding of the two PDMS layers, resulting in slight mismatches between C1 and C2 (Fig. 2a). To alleviate mismatch caused by alignment error, the first robust design strategy places extra valves on the dummy channels connected to C2 (Fig. 2c). During operation of the DAC, extra valves are closed, thus guaranteeing identical channel lengths connected to both capacitors under y alignment errors and only small errors under x alignment errors.

Other than mismatch, volume injection from S3 actuation can also result in output nonlinearity (Fig. 3a). This nonlinearity can be understood as a vertical offset in transfer function resulted from extra volume of liquid pushed into a PDMS chamber and deforming the capacitive membrane. The second robust design strategy uses a method similar to top plate cancelation in IC design, we add valves to both sides of C1 and C2 (Fig. 3ab). S6 is always closed while S7 assumes the opposite state of S3, creating extra volume to accommodate injected fluids. Even though the proposed volume injection compensation design requires more stringent x alignment to function perfectly, small x errors would still alleviate injection. In addition, the addition of S6 and S7 decreases the sensitivity of capacitive mismatch to x alignment errors.

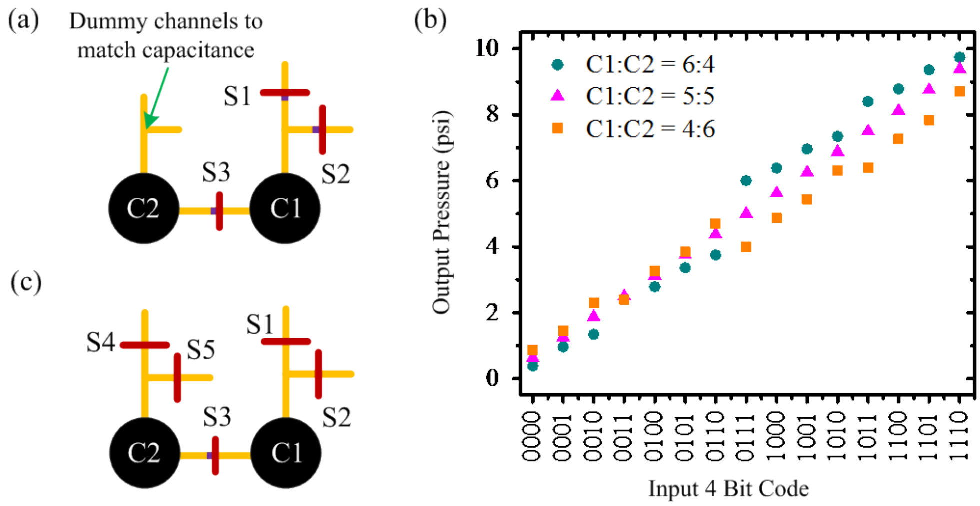

Figure 2: Alignment error insensitive design using dummy valves. (a) Alignment errors in x and y result in mismatched capacitances (purple) when fixed dummy channels are used to mirror design geometry (green arrow). (b) Simulation show that mismatched capacitors result in nonlinearity in output transfer function of the microfluidic DAC. (c) Adding dummy valves S4 and S5 reduces possible mismatch between C1 and C2. Y alignment errors now have no effect on capacitive mismatch.

EXPERIMENTAL

To test the applicability of the proposed design strategies, we fabricate a new version of the microfluidic serial DAC including dummy channels on C2 and dummy valves S4, S5, S6, and S7 (Fig. 3b). This device is fabricated using standard multilayer soft lithography technique. First, molds are created for each PDMS layer. A positive photoresist SPR is used to pattern the flow channels whereas control channels and capacitive chambers are patterned out of SU8, a negative photoresist. Then, PDMS is molded layer by layer and bonded from top to bottom. Testing of the device is performed on a Leica DMI 6000 inverted microscope. The center displacement of the capacitive diaphragm is monitored and translated into a pressure applied to the membrane. The translation is obtained through calibration. After obtaining the pressure applied to the C2 diaphragm, the DAC transfer function can be plotted.

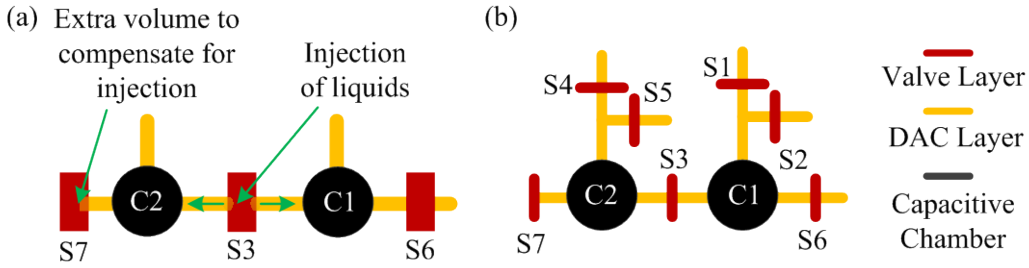

Figure 3: Improved design for volume injection correction. (a) When S3 closes, some volume of incompressible fluid is displaced into C2, increasing output pressure. S7 opens when S3 closes to accommodate volume injection. (b) The final improved design is insensitive to small x y alignment errors and corrects for volume injection.

RESULTS AND DISCUSSION

In order to make the comparison meaningful, three improved devices with the same diaphragm diameter are tested. When the input-output transfer functions of the new devices (Fig. 4a) are compared to the original transfer functions (Fig. 4b), it can be seen that the linearity of microfluidic DACs designed using the proposed robust design strategies is far superior to the DACs without using such design strategies. In the original DAC transfer functions, vertical kinks are most likely due to capacitive mismatch. According to simulation, when C1 > C2, transfer functions display vertical discontinuities when the MSB (Most Significant Bit) changes from 0 to 1. This is consistent with the fact that C1 has more channels connected to it. Another observation from the original DAC transfer functions is that when the diameter of the capacitive membrane decreases, the transfer function seems to display larger vertical offset. This phenomenon is related to a smaller capacitance associated with smaller diameter membranes showing a larger effect under volume injection. In contrast, transfer functions of the improved DACs all have more linear transfer functions. More importantly, the transfer functions do no depend on membrane diameters as long as the C1 and C2 have the same membrane diameter.

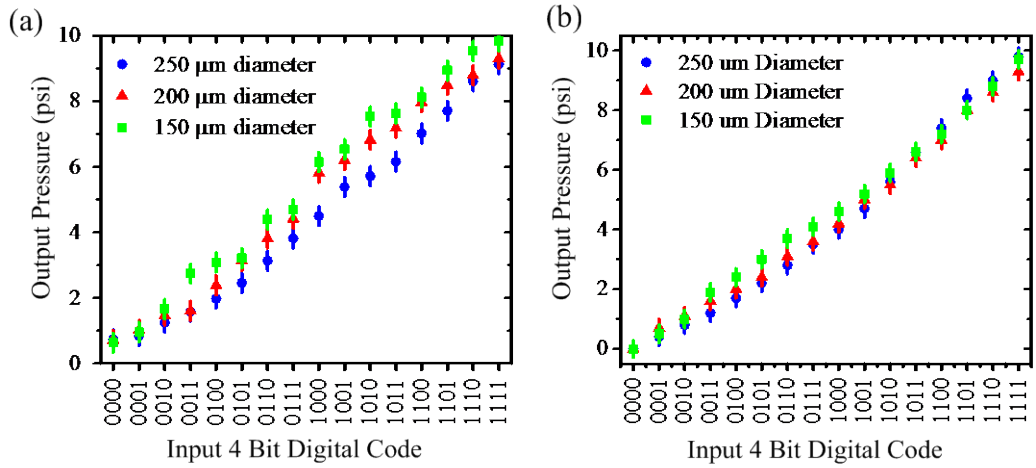

Figure 4: Comparison of the microfluidic DAC performance before (a) and after (b) implementing the new design demonstrates significant improvements in output linearity. In fact, with better matched capacitors and correction for volume injection, we see that the DAC output is independent of membrane diameters.

CONCLUSION

Using the proposed robust design strategies explained previously, new versions of the microfluidic serial DAC are fabricated and display more linearly transfer functions (Fig. 4). In addition, output is no longer dependent upon size of the capacitive membranes. Even though such a design increases the number of fluidic connections, we believe these techniques will be useful to any complex multilayer PDMS microfluidic devices whose functionalities are sensitive to volume injection or depend on matched capacitances.

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