CMOS-INTEGRATED HIGH-DENSITY ARRAYS OF CARBON NANOTUBE SENSORS

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ABSTRACT

We report on the integration of single and small bundles of carbon nanotube (CNT) biosensors on a CMOS-integrated array featuring 1024 devices. The system has been designed to allow for direct and versatile readout of each nanosensor. A parallel integration of the CNT nanosensors has been achieved by using semi-sacrificial electrodes and dielectrophoresis (DEP). The developed sensing platform will be used for high-resolution chemical monitoring of complex biological systems. Here, we present the on-chip CNT integration process and statistical analysis of the fabricated devices.

KEYWORDS: Carbon nanotube, nanosensors, CMOS, dielectrophoresis

INTRODUCTION

CNTs have been shown to be a highly efficient and versatile material for the fabrication of nano-biosensors [1]. Single CNT sensors have been successfully used for the sensing of molecular events, such as interaction with complementary ss-DNA [2], or the detection of single protein kinetics [3]. The use of CNT sensing material in integrated systems is challenging due to the lack of CMOS-compatible fabrication processes. Previously, low-density CMOS integration of sensors based on a large number of parallel CNTs has been reported [4]. Nevertheless, the yield and performance remained low, and elaborate integration methods had to be used. We present here a new approach for the integration of single or small bundles of CNT nanosensors on a high-density sensor array (≥ 100 sensors/mm^2).

EXPERIMENTAL

As a platform we used CMOS chips, fabricated in 0.35µm, 2P4M technology, previously reported at IEEE Sensors 2012 [5]. This chip includes an array of 32x32 pixels, which can be individually monitored by 64 current-mode readout channels. An additional Pt layer and a thick SiO_2/Si_3N_4 passivation layer stack were used to protect the CMOS circuitry against the liquid environment during sensing (Figure 1a).

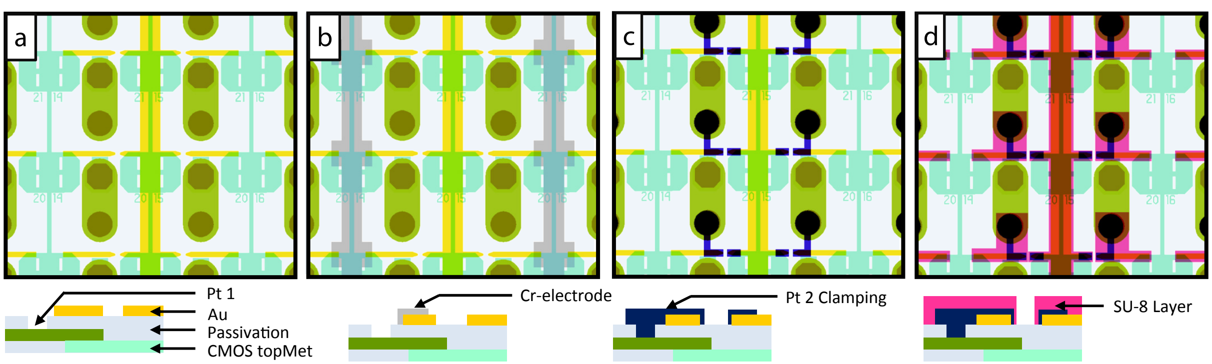

Figure 1: Semi-sacrificial DEP integration process. a. Top view of a subset of the array with Pt, SiO_2/Si_3N_4 passivation and Au-electrodes. b. Cr-electrodes. c. Pt clamping and connection to CMOS circuitry. d. SU-8 insulating layer.

The CNTs were integrated by using a positive DEP protocol. An array of disconnected Au-electrode pairs was patterned on the chip by using photolithography. Cr-electrodes interdigitated to the Au electrodes were patterned to connect these Au electrode pairs. This design allowed for the generation of precisely localized, high electric field gradients (Figure 1b,c; Figure 2a,b). A 300kHz and 1Vpp/µm electric field was used to create positive DEP forces on CNTs dispersed in a water-based suspension (synthetized by Catalytic CVD, Double-wall CNT, dispersed with Carboxymethyl cellulose [6]). The Cr-electrodes were then selectively etched to create independent devices (Figure 2c). A metallization step was used to clamp the CNTs to the electrodes and to connect them to the CMOS circuits (Figure 1d; Figure 2d). Finally, a SU-8 layer was added to protect the metal layers from the environment (Figure 1d; Figure 2e).

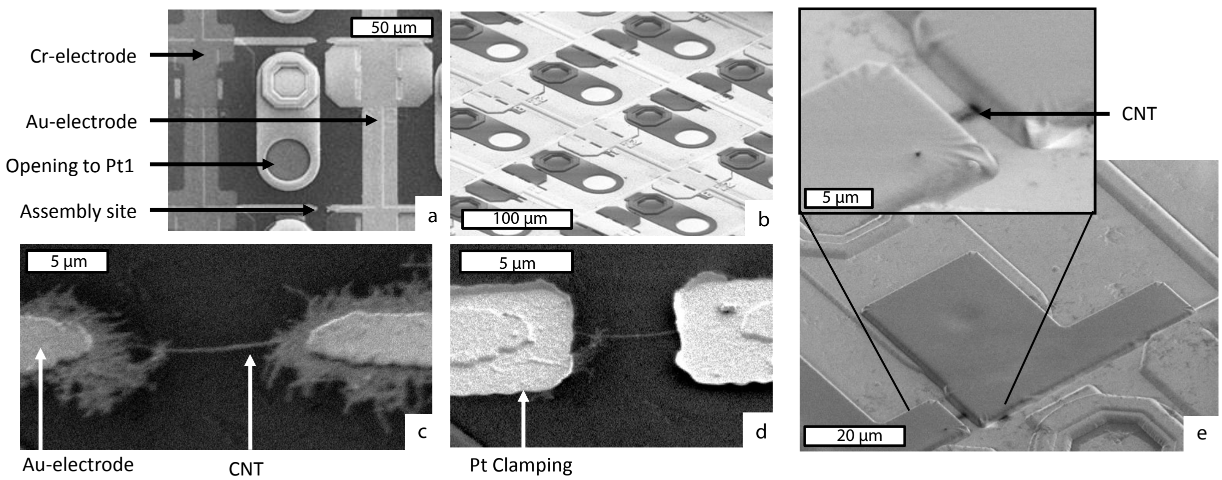

Figure 2: Scanning electron microscopy (SEM) images of the integration process. a. One pixel showing the DEP electrodes. b. Array overview. c. Au-electrodes and CNT assembly by DEP. d. Same CNT device after Pt clamping. e. Final device after protective-layer patterning.

RESULTS AND DISCUSSION

The optimization of the integration process has been monitored by using voltage-contrast SEM [7] and direct SEM imaging (Figure 4a,b). Our integration process yielded about 54% CNTs connected to pairs of electrodes, out of which 45% were single nanodevices (single CNTs or small bundles). After Pt clamping and addition of the final passivation layer, the CNT nanosensors were electrically characterized by using the CMOS circuitry (Figure 4c,d). The parallel readout and resistance measurement of a subset of preselected CNT devices is presented Figure 4c and 4d.

CONCLUSION

We have presented a process for the integration of CNTs as sensing elements with CMOS circuits. This work represents a significant improvement of integration rate, density, and number of "single" CNT devices on CMOS circuits with respect to previous work. The presented CMOS-based platform is under test for applications, such as local detection of biochemical substances and highly sensitive multiplexed sensing.

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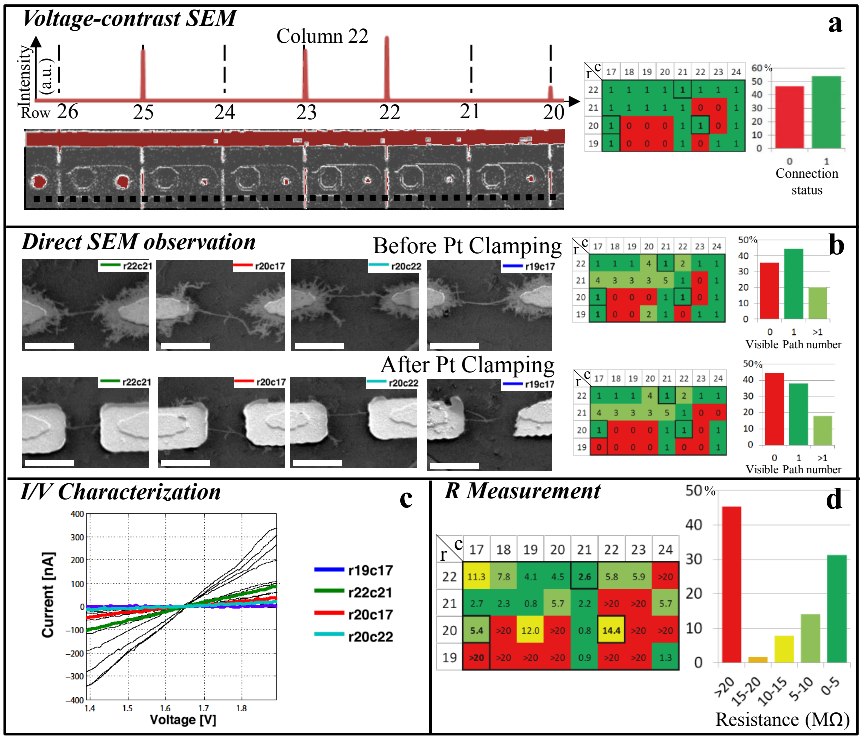

Figure 3: Characterization of the devices. a. Voltage-contrast SEM analysis of a sub-array. b.(Top) SEM analysis of selected CNT connections after DEP (scale bar 5µm) (Bottom) Direct SEM observation data of a sub-array: CNT connections after Pt clamping (scale bar 5µm). (r19c17 is broken) c. I-V characteristics of all devices of the sub-array. d. Resistance measurements of the sub-array.

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