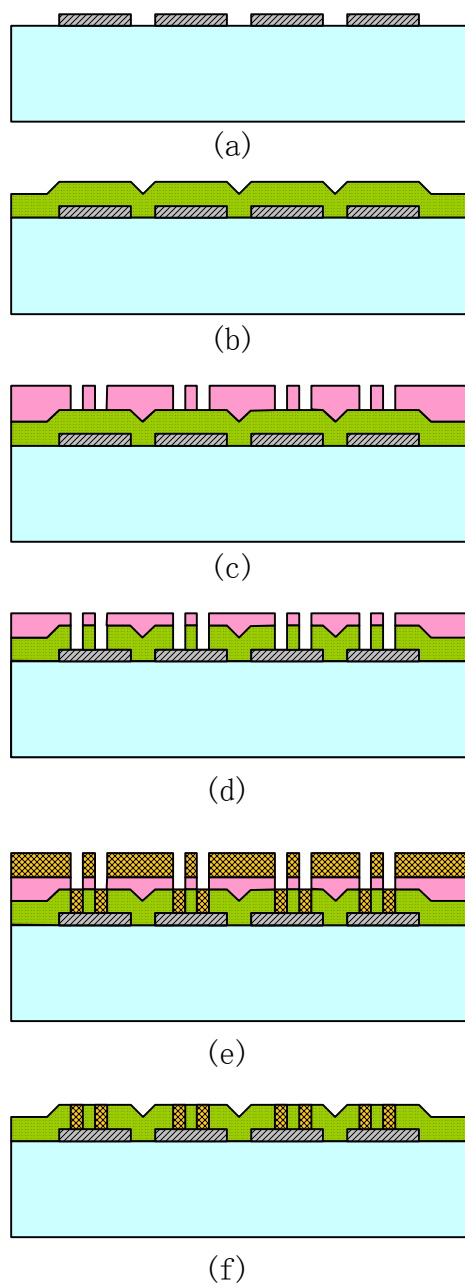


### Supplementary Materials



Supplementary Figure 1. Schematic showing the process to make a nanoscale electric lithographic mask (a) 20 nm thick Cr sub-micron patterns are made by e-beam lithography on a glass substrate as the electric connections to nanoscale patterns; (b) A 50 nm thick SiO<sub>2</sub> electrically insulative layer is deposited all over the substrate; (c) Nanoscale openings are made in an e-beam resist layer by e-beam lithography; (d) Nanoscale openings are made in the SiO<sub>2</sub> layer by using the e-beam resist as etching mask in reactive ion etching; (e) A 50 nm thick Au layer is deposited by an e-beam evaporator; (f) A "lift-off" process is used to remove the e-beam resist and define the nanoscale Au patterns on the mask.