Supplementary Information

for

Surface grafting of octylamine onto poly(ethylene-alt-maleic anhydride) gate insulators for low-voltage DNTT thin-film transistors

Yun-Seo Choe,ab Mi Hye Yi,a Ji-Heung Kim,b Yun Ho Kim,*a and Kwang-Suk Jang*a

aDivision of Advanced Materials, Korea Research Institute of Chemical Technology, Daejeon 34114, Republic of Korea. E-mail: kjang@kRICT.re.kr, yunho@kRICT.re.kr

bSchool of Chemical Engineering, Sungkyunkwan University, Suwon 16419, Republic of Korea
1) Al deposition using thermal evaporation

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Gate (Al)
Substrate (SiO₂/Si)
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2) Spin-coating of PEMA gate insulator

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PEMA gate insulator
Gate (Al)
Substrate (SiO₂/Si)
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3) Octylamine treatment by spin-coating

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Octylamine
PEMA gate insulator
Gate (Al)
Substrate (SiO₂/Si)
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4) DNTT deposition using thermal evaporation

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DNTT
Octylamine
PEMA gate insulator
Gate (Al)
Substrate (SiO₂/Si)
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5) DNTT deposition using thermal evaporation

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Source (Au)  Drain (Au)
DNTT
Octylamine
PEMA gate insulator
Gate (Al)
Substrate (SiO₂/Si)
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Fig. S1 Scheme of the TFT device fabrication.
Fig. S2 The surface coverage measurement of the 12 nm-thick DNTT layers on non-treated and octylamine-treated PEMA thin films.
**Fig. S3** Transfer characteristic ($I_{ds}$ vs. $V_{gs}$) of the DNTT TFTs with the 60 nm-thick SiO$_2$ gate insulator.