Electronic Supporting Information

Origin of Grain Boundary Capacitance in Highly Doped Ceria

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Figure S-1. Energy band diagram of bulk-grain boundary interface in a reduced doped ceria electrolyte showing the Ce\textsuperscript{III}\textsuperscript{::}4f\textsuperscript{1} electrons firstly introduced into the grains (a) followed by charge transfer to the grain boundary phase, leading to the formation of a depletion space-charge layer at the bulk-gb junction (b).
– Instrumentation for electrical measurements

The following picture illustrates the impedance reactor constructed to perform impedance measurements under reducing atmosphere.

![Diagram of the experimental setup](image)

**Figure S-2.** Schematic of the experimental set up employed to study the electrical behavior of samarium doped ceria under different pO$_2$ and temperature.