Electronic Supplementary Material (ESI) for Nanoscale.

Supporting Information

Self-screened high performance multi-layer MoS_2 transistor formed by using bottom graphene electrode

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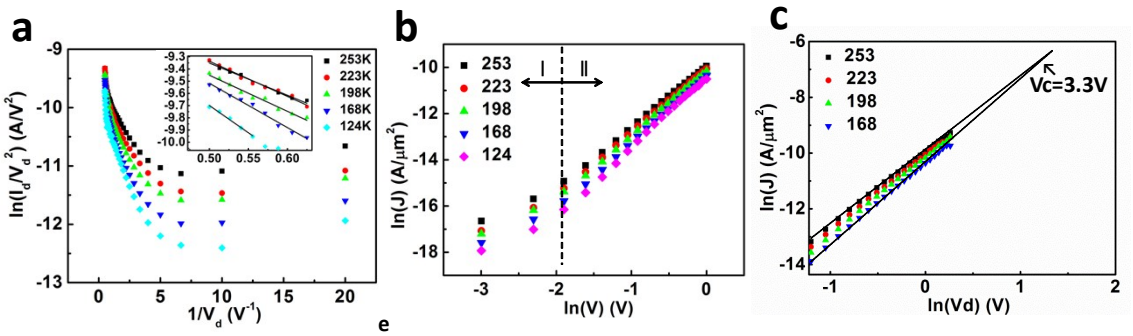
S1 (Space charge limited conduction in other device)



S2 (AFM image of our device)

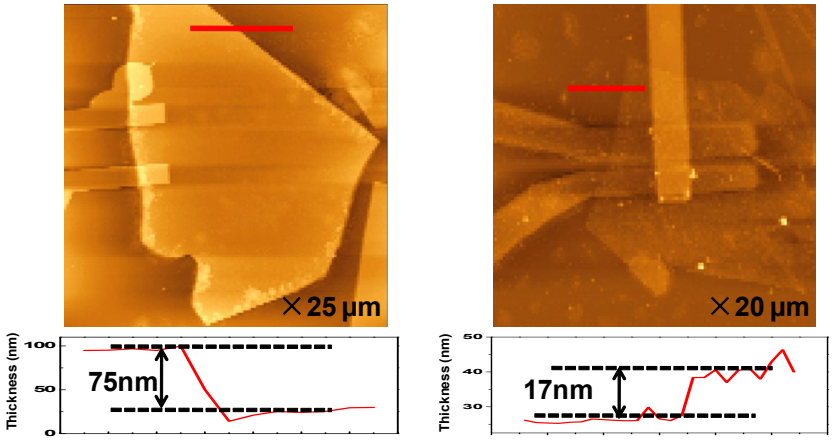


Figure S2, Atomic force microscope image of our devices and corresponding flake thickness. 75nm bottom graphene contacted device and 17nm vertically stacked metal/MoS_2/metal device are shown above.

S3 (thickness-dependent transfer curves of top Cr/Au contacted devices)

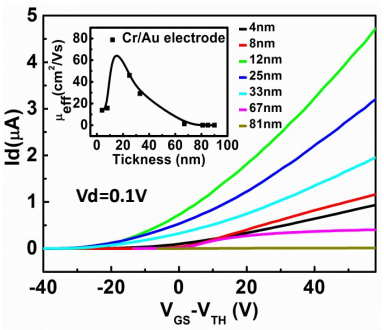


Figure S3, Thickness-dependent transfer characteristics of the MoS_2 transistors prepared with conventional metal contacts. The inset shows the mobility extracted from the transfer curves.

S4 (Metal-Insulator transition in bottom graphene contacted device)

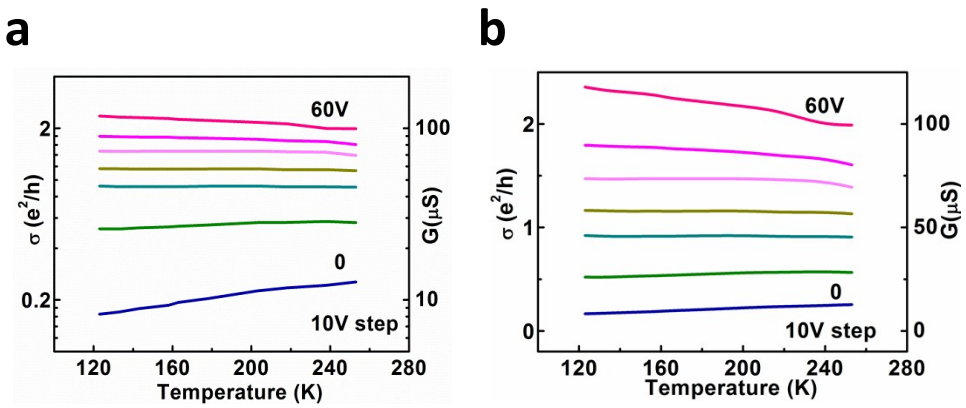
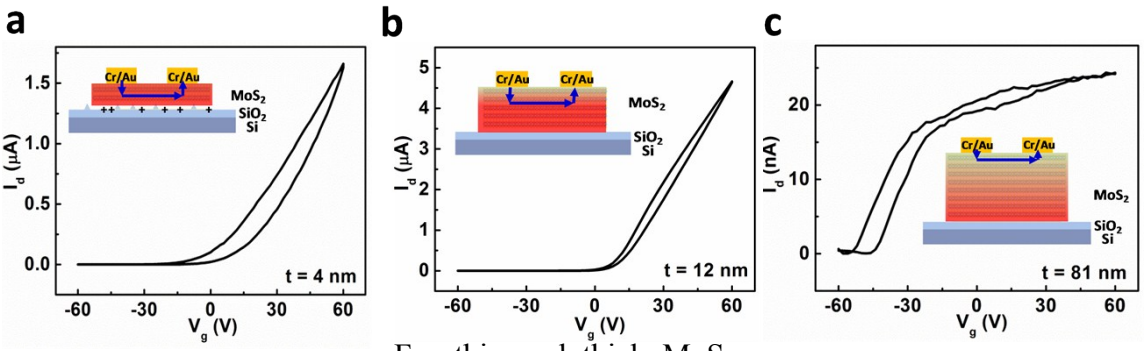


Figure S4 a, Logarithmic scale of temperature dependent conductivity and conductance of 75nm bottom graphene contacted device, showing a metal–insulator transition. **b**, Linear scale of temperature dependent conductivity and conductance, the decreasing trend of conductivity at high gate voltage indicates metallic property of MoS_2 at this region.

These results demonstrated that MoS_2 behaved as a typical semiconductor, in which the conductance decreased as the temperature decreased for a gate voltage of < 30 V. Under higher applied gate voltages, the conductivity increased with decreasing temperature, indicating that the channel MoS_2 entered a metallic state with a critical $\sigma \sim e^2/h$. The value of e^2/h is equal to the minimum metallic conductivity, which is not thought to exist in 2D electronic systems, according to the scaling theory of localization based on non-

interacting electronic gases. This observation indicated that a metal–insulator transition (MIT) occurred in our two-terminal device. This transition usually goes undetected due to the masking effects of the Schottky barrier at the contact. The transition could be observed, however, using a four-terminal measurement set-up that excluded the contact resistance, as the conductance at a Schottky barrier-dominated device decreased at lower temperatures due to reduced thermal emission. So the observation of MIT was also an indication of excellent contact in our device.

S5 (hysteresis of MoS_2 FET at different thickness)



For thin and thick MoS_2 FET, carrier transport are limited to the bottom and top few layers respectively as shwon in the inset of figure S4a and S4c. Large hysteresis of transfer curves were observed from both thin (4 nm) and thick (81 nm) MoS_2 FET, indicating scattering or charge traps from substrate or contamination in top layers. 12 nm MoS_2 flake tended to show the best performance as indicated in figure S3, it however still showed non-negligible hysteresis as shown in figure S5b.