Supplementary Information

Phase-driven Magneto-electrical Characteristics of Single-layer MoS₂

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Fig. S1: The CVD-prepared MoS₂ isolated domains were transferred to fresh SiO₂/Si substrates for device fabrications. Au electrode patterns as source and drain were prepared by E-beam lithography technique followed by E-gun evaporation deposition. The pattern layout is illustrated in this figure. The SiO₂/Si substrates were employed as dielectrics and back gate respectively for controlling the carrier concentration of MoS₂ channel. The transport properties were investigated with Keithley 4200 semiconductor characterization system. The same FET devices were examined before and after gas treatments for comparison.
Fig. S2: The electrical characteristics ($I_d$-$V_g$) measured at $V_d=1$ V, for (a) pristine, (b) O$_2$-treated, and (c) Ar-treated MoS$_2$ FET. All of the device conditions show an n-type behavior. The corresponding $I_{on}/I_{off}$ ratio and mobility ($\mu$) of respective device condition are numerically demonstrated inside the figures.