Automated Characterization and Assembly of Individual Nanowires for Device Fabrication

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Supporting Information

[supplementary document doi]

1. Motion control of nanowires using electrode array in fluid suspension [1]

In order to scalable manipulate of nanostructures, a simple and generic set of $N \times N$ lattice-shape distributed electrode array is designed to actuate suspended nanowires under electric-fields in fluid suspension. The precisely controlled electric fields generated by electrode arrays can be used to control the motion of nanowire. The nanowire motion is modeled as that of a non-spherical particle immersed in a viscous fluid under external electric field. Under a DC electric field, the equation of motion for one nanowire is given as

$$\dot{\boldsymbol{r}}_i = \begin{bmatrix} v_{ix} \\ v_{iy} \end{bmatrix} = \frac{\varepsilon_{\mathrm{m}} \zeta_i \boldsymbol{E}_i}{\mu_{\mathrm{m}}} = C_i \begin{bmatrix} E_{ix} \\ E_{iy} \end{bmatrix}, \tag{S1}$$

where the position of the ith nanowire is denoted as $\boldsymbol{r}_i(t) = [x_i(t)\ y_i(t)]^T$, $i = 1, \cdots, n$. $\boldsymbol{E}_i = [E_{ix}\ \ E_{iy}]^T$ is the DC electric-field vector at $\boldsymbol{r}_i$, $C_i = \varepsilon_{\mathrm{m}} \zeta_i / \mu_{\mathrm{m}}$, μ_{m} is the dynamic viscosity, and ε_{m} is the electric permittivity. ζ_i is the zeta-potential of the ith suspended particle and is estimated online for each nanowire. The $\boldsymbol{E}_i$ can be calculated by superposition of effective electrodes with *unit* voltage and u_j, $j = 1, \cdots, N^2$, is the corresponding voltage that is applied on the $N \times N$ electrode array. From Equation (S1), the electric field is regulated to steer the nanowires' motion by appropriately applying voltage to electrodes.

To formulate the motion equations for all n nanowires, we first re-index the electrodes into a one-dimensional N^2-element array with a column-wise order. We denote the electric field under unit voltage at $\boldsymbol{r}_j(t)$ by the ith electrode as $\boldsymbol{E}_i(\boldsymbol{r}_j(t)) = [E_{x_i}(\boldsymbol{r}_j(t))\ E_{y_i}(\boldsymbol{r}_j(t))]^T$, $j = 1, \ldots, n$, and the corresponding controlled electrode voltage as $\boldsymbol{u}_{\mathrm{c}} = \{u_j\} \in \mathbb{R}^{N^2}$.We also concatenate the position vectors of all nanowires as $\boldsymbol{q}(t) = [\boldsymbol{r}_1^T(t) \cdots \boldsymbol{r}_n^T(t)]^T \in \mathbb{R}^{2n}$. By defining a *motion gain matrix*

$$\boldsymbol{B} = \begin{bmatrix} C_1 \boldsymbol{E}_1(\boldsymbol{r}_1(t)) & \cdots & C_1 \boldsymbol{E}_{N^2}(\boldsymbol{r}_1(t)) \\ \vdots & \ddots & \vdots \\ C_n \boldsymbol{E}_1(\boldsymbol{r}_n(t)) & \cdots & C_n \boldsymbol{E}_{N^2}(\boldsymbol{r}_n(t)) \end{bmatrix}, \tag{S2}$$

we re-write Equation (S1) for all nanowires as

$$\dot{\boldsymbol{q}} = \boldsymbol{B} \boldsymbol{u}_{\mathrm{c}}, \tag{S3}$$

where $\boldsymbol{B} \in \mathbb{R}^{2n \times N^2}$. Every two rows in Equation (S3) represent one nanowire's equation of motion.

Given the desired velocity $\dot{\boldsymbol{q}}_d$, a least-square problem is formulated to obtain control input $\boldsymbol{u}_{\mathrm{c}}$ in Equation (S3)

$$\begin{aligned} \min_{\boldsymbol{u}_{\mathrm{c}}} \quad & \|\boldsymbol{B}\boldsymbol{u}_{\mathrm{c}} - \dot{\boldsymbol{q}}_{\mathrm{d}}\|_2 \\ \text{subject to} \quad & u_{\min} \leq \|\boldsymbol{u}_{\mathrm{c}}\|_\infty \leq u_{\max}, \end{aligned} \tag{S4}$$

where $u_{\min}$ and $u_{\max}$ are respectively the lower- and upper-bound of the applied voltages. A quadratic programming technique is used to solve Equation (S4).

Fig. S1 shows the schematic of the micro-fluidic device with $N \times N$ electrodes on the bottom surface. The array of circular electrodes with radius R are fabricated on a glass substrate with equal distance L between centers. Each electrode is independently actuated with a DC voltage. The electrode arrays are covered by fluid containing a dilute concentration of nanowires. A glass coverslip is used to cover the fluid and form a flow reservoir.

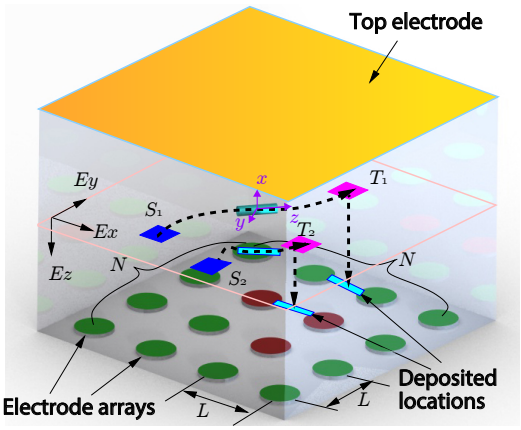


Fig. S1. Schematic of microfluidic device with $N \times N$ electrodes independently actuated electrodes on the bottom substrate, with a common top electrode.

2. Simultaneous multiple-nanowire contactless and solution-based electro-orientation spectroscopy (EOS)

When applying electric fields to the liquid suspension, a torque is exerted on the nanowire, under which the nanowire tends to align with the electric field. This effect, called electro-orientation, works for both DC and AC fields, and it is irrespective of the spatial uniformity of the electric field. The EOS mentioned in the paper is based on the electro-orientation principle [2, 3]. Under non-uniform electric field, nanowires at different locations may experience different electric fields. In planar motions, the exerted torque about the x-axis that is perpendicular to the horizontal plane can be expressed as

$$|\boldsymbol{\tau}| = \pi a b^2 \varepsilon_{\mathrm{m}} E_0^2 \sin(2\theta)\, \mathbf{Re}[\underline{\kappa}], \tag{S5}$$

where

$$\underline{\kappa} = \frac{\underline{\varepsilon}_{\mathrm{p}} - \underline{\varepsilon}_{\mathrm{m}}}{3[\underline{\varepsilon}_{\mathrm{m}} + (\underline{\varepsilon}_{\mathrm{p}} - \underline{\varepsilon}_{\mathrm{m}})L_{||}]}, \tag{S6}$$

$\underline{\varepsilon}_{\mathrm{m}}$ and $\underline{\varepsilon}_{\mathrm{p}}$ are the complex permittivity of the fluid and the particle, respectively, and ε_{m} is the real part of the fluid permittivity $\underline{\varepsilon}_{\mathrm{m}}$. E_0 is the magnitude of the AC electric field $\boldsymbol{E}$.

From Equation (S5), it is clear that the rotation alignment rate depends on the electric field strength, and the orientation of the nanowire tends to align with the electric field direction. In addition, the induced dipole moment of the particle can interact with the non-uniform field to give rise to a frequency-dependent DEP force. The DEP force is proportional to the polarizability of the particle and the gradient of the field squared [4], namely,

$$\langle \boldsymbol{F}_{\mathrm{DEP}} \rangle = 2\pi a b^2 \underline{\varepsilon}_{\mathrm{m}}\, \mathbf{Re}[\underline{\kappa}] \nabla \boldsymbol{E}_{\mathrm{rms}}{}^2, \tag{S7}$$

where a and b are the semi-major and semi-minor axes of the prolate spheroid, respectively. The DEP force would result in translation of the nanowires in the suspension. In order to enable the capability of characterizing multiple nanowires simultaneously using the EOS principle, a pair of parallel electrodes are designed to generate uniformly distributed AC electric fields. Ideally, the uniformly distributed field only generates electro-orientation, *i.e.*, no DEP-induced translation motion. The rotation alignment rate of each nanowire is not affected by the variations of electric fields. Therefore, the extracted conductivities of multiple nanowires by their alignment rates are comparable, which can be utilized as the separation criterion. Another reason for not using the electrical field generated by the assembly electrode array design presented in [1, 5] is that, in real time, it is difficult to calculate the exact electric field at a given location to compensate for the inaccurate EOS measurement due to the electric field-induced orientation and translation.

3. Automation process of the ACMAN design

The characterization, manipulation, and assembly processes are all automated. Fig. S2 shows the schematic of the complete automated system. The microfluidic device containing nanowire suspension is installed on a motorized, computer-controlled microscope XY stage (Prior ProScan III) on an inverted microscope (Olympus IX71). Bright field images are recorded using a low light high sensitivity camera (pco.edge sCMOS). The high-resolution images provide real-time visual feedback of the precise movements of the nanowires in larger range of motion for the online motion controller. An embedded system (NI cRIO 9074) is used as distributed motion control to actuate the electrode array and a LabView application extracts nanowire positions in real time from recorded images and provides visualization system in a desktop computer.

The human operator needs to specify the separation criterion with the target deposition areas (where to deposit the two groups of nano-particles according to the separation criteria), and selects the nanowires of interest to be analyzed and manipulated in the visualization system. Then, the real-time image segmentation is conducted to obtain orientation and position of the nanowires. Next, the automated system shown in Fig. S2 manipulates and characterizes the nanowires, tracks their motions, and assembles them according to the separation criteria. Fig. S3 shows the flow chart of the ACMAN process. In the current developed software application, the operator needs to manually adjust the focus plane as the nanowires changing z-position. An auto-focus feature can be developed in the future.

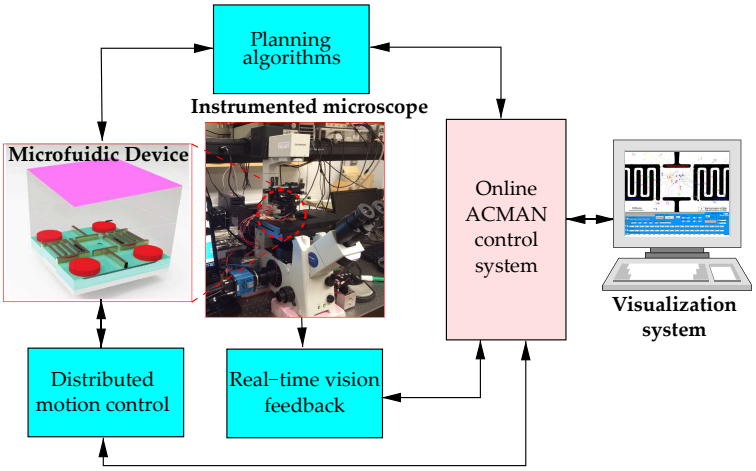


Fig. S2. *A schematic of the electric-field-based nanowires characterization, manipulation, and assembly scheme in a completely online and automated manner.*

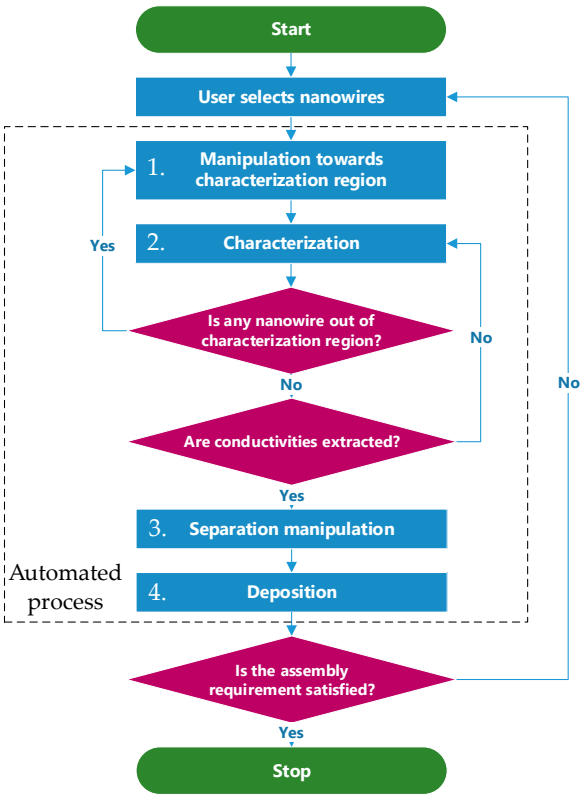


Fig. S3. Flow chart of the integrated ACMAN system. Dashed box shows the automated process.

4. Supplementary measurement data on automated assembly of Si NW-based FETs using ACMAN

A. Characteristics and performance of the FET devices fabricated using ACMAN

The current-voltage characteristics of the ACMAN assembled Si NW transistors are measured using an HP 4140B Picoammeter semiconductor analyzer system with probe station. The transfer characteristics of ACMAN-assembled Devices 1 to 4 are shown in Figs. S4 - S7, respectively.

ACMAN Device 1 contains a total of 24 Si NWs, where 12 nanowires (NWs) were characterized, selected, and deposited on the desired locations according to their conductivities. However, the resulting FETs had 10 NWs remaining on each side after the wrap-around electrode fabrication by the metal lift-off process. Both FETs of ACMAN Device 1 show n-type characteristics. The FET constructed by the high-conductivity (HC) NWs shows two orders of magnitude higher current in the device on-state than the FET with the low-conductivity (LC) NWs as shown in Fig. S4(a). Fig. S4(b) shows the measured electrical conductivity distribution of the separated and deposited 24 Si NWs using the simultaneous multiple-nanowire EOS. The red dash-line represents the separation

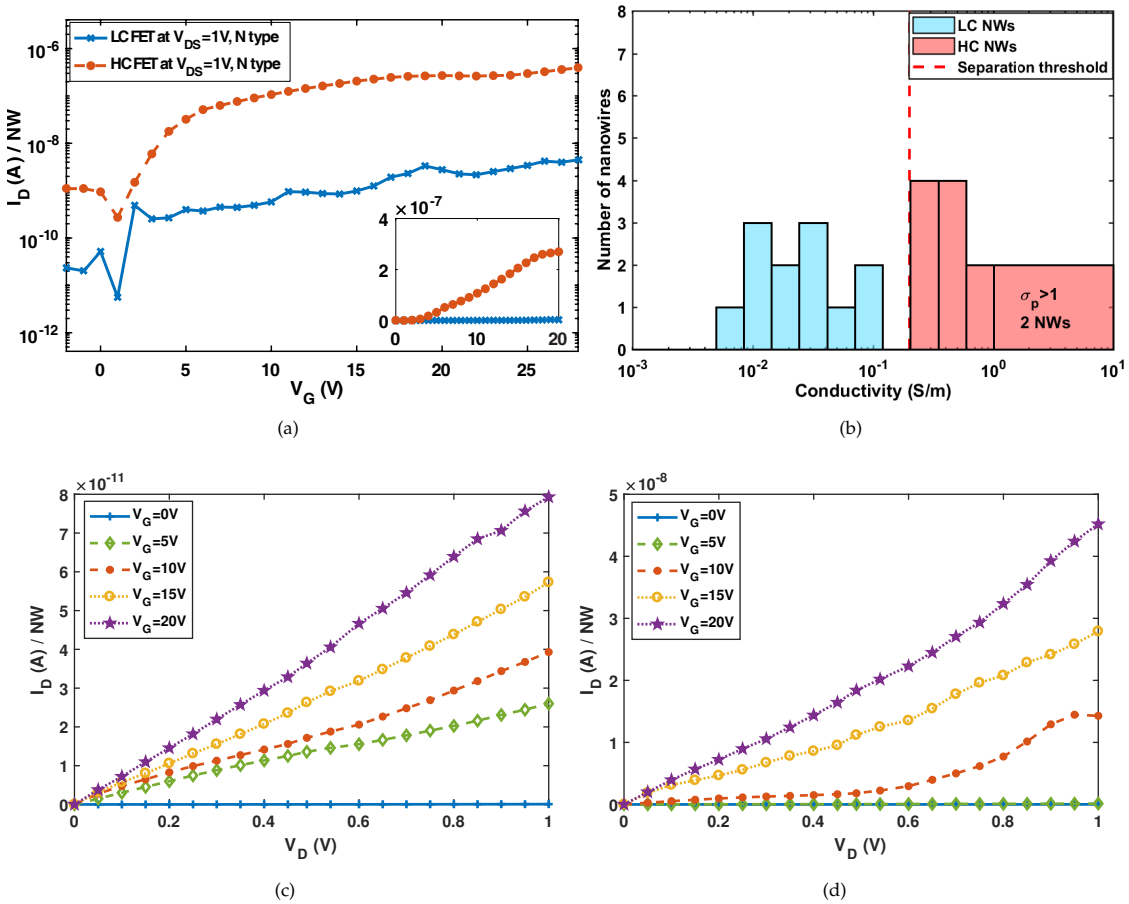


Fig. S4. ACMAN Device 1: A proof-of-concept demonstration of the integrated ACMAN process to assemble Si NWs as FET devices. A total of 24 Si NWs was initially deposited, with 12 nanowires (NWs) characterized and deposited on the high-conductivity (HC) and the low-conductivity (LC) sides according to their electrical conductivities, respectively. After the wrap-around electrode fabrication, the resulting FETs have 10 NWs on each side, showing n-type characteristics. (a) Transfer characteristics in logarithmic scale showing the drain current per nanowire at source-to-drain voltage $V_{DS} = 1$ V for the two n-type FETs after separation. Inset: The transfer characteristics in linear scale. (b) Measured electrical conductivity distribution against the number of characterized nanowires by EOS. (c) Output characteristics of the LC FETs showing the drain current per nanowire at gate voltage $V_G = 0$ to 20 V in 5 V steps. (d) Output characteristics of the HC FETs showing the drain current per nanowire at $V_G = 0$ to 20 V in 5 V steps.

threshold $\sigma_{th} = 0.2$ S/m. In the experiment, one or two NWs were characterized, separated, and deposited at one time due to the electrode array dimension. Figs. S4(c) and S4(d) illustrate the output characteristics of the FETs in the LC and the HC sides, respectively. The output characteristics show an almost two-order difference between the two FETs. This result is consistent with the transfer characteristic and the conductivity distribution measurements.

Figs. S5 to S7 show the characteristics and performance of the ACMAN Devices 2 to 4. For the ACMAN-assembled Device 3, a total of 20 Si NWs were initially deposited, with 10 NWs selected and positioned on each side according to their electrical conductivities. Fig. S6(b) shows the measured electrical conductivity distribution of the 20 Si NWs that were characterized and separated using simultaneous multiple-nanowire EOS. After the wrap-around electrode fabrication, 3 NWs remained on each side in the channel gap. The FET made with selected HC NWs shows n-type characteristics, while the LC side demonstrates p-type characteristics. The corresponding output characteristics of the FETs in the LC and the HC sides are shown in Figs. S6(c) and S6(d), respectively.

As shown in Figs. S5 and S7, ACMAN Devices 2 and 4's characteristics also confirm the effectiveness of the integrated ACMAN scheme and yield the HC Si NW-based FETs with at least one order of magnitude higher on-current as compared to the LC Si NW-based FETs. The corresponding output characteristics and the conductivity distribution measurements substantiate similar conclusion.

B. Measurement characteristics of the FET devices fabricated using DEP-only technique

Fig. S8 illustrates the characteristics of the FET device fabricated using the DEP-only assembly scheme. Si NWs were collected at different DEP frequencies. 2 MHz and 20 kHz frequencies with 50 V_{pp} AC fields are used to fabricate the HC and LC FETs, respectively, which are the same fields as used in the deposition step to trap nanowires for ACMAN-assembled devices. For each DEP-only device, AC fields are applied until at least 30 NWs were trapped in both sides of the electrodes gap (the HC side would have about 30 NWs, while the LC side would attract far more then 30 NWs for the chosen frequencies) to maintain similar amount of NWs as ACMAN

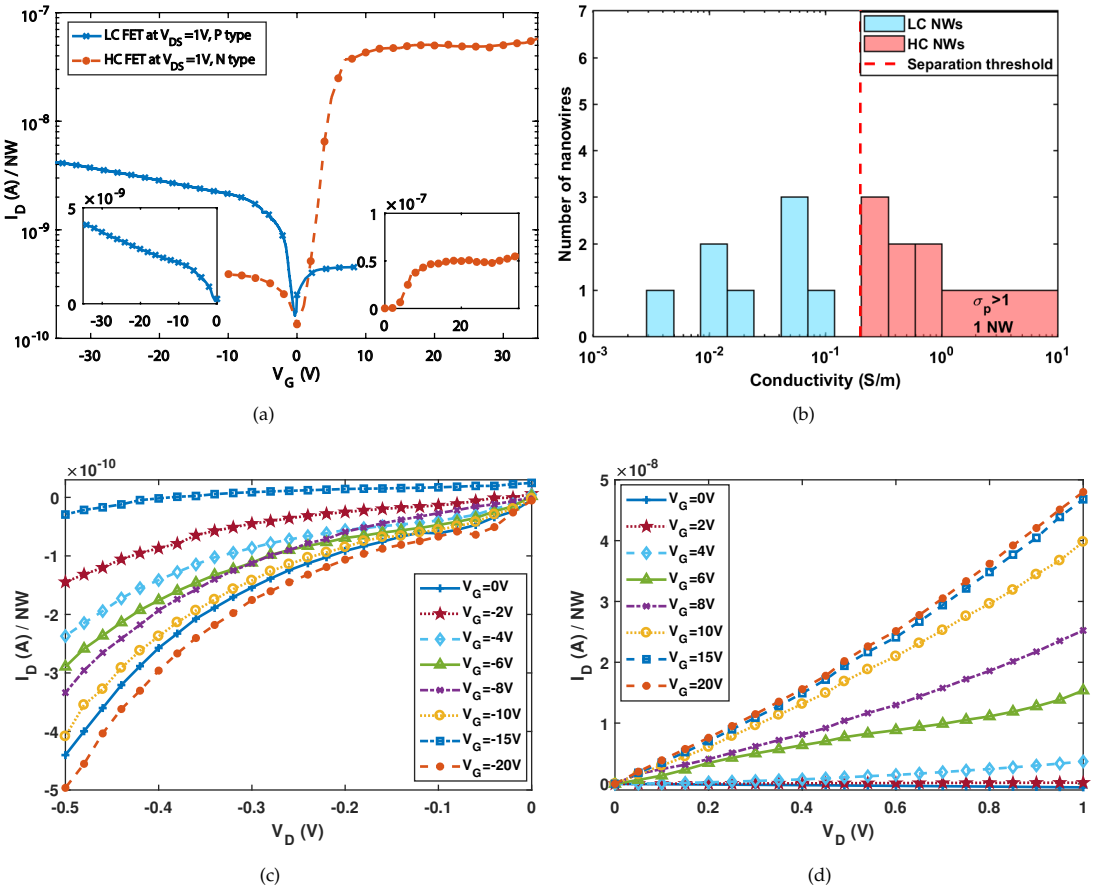


Fig. S5. ACMAN Device 2: A proof-of-concept demonstration of the integrated ACMAN process to separate and assemble of 16 Si NWs into FET devices. A total of 16 Si NWs was initially deposited, with 8 NWs characterized and deposited on the HC and the LC sides, receptively. After the wrap-around electrode fabrication, the resulting FETs have 3 NWs on each side. The FET assembled with LC Si NWs shows p-type characteristics while the FET assembled with HC Si NWs shows n-type characteristics. (a) Transfer characteristics in logarithmic scale showing the drain current per nanowire at $V_{\mathrm{DS}} = 1$ V for the p-type and n-type FETs after separation. Inset: The transfer characteristics in linear scale. (b) Measured electrical conductivity distribution against the number of characterized nanowires by EOS. (c) Output characteristics of the LC FETs showing the drain current per nanowire at $V_{\mathrm{G}} = 0$ to -20 V. (d) Output characteristics of the HC FETs showing the drain current per nanowire at $V_{\mathrm{G}} = 0$ to 20 V.

devices through the metal wrap-around photo-lithographic process.

C. Performance metrics of the fabricated FET devices

To quantitatively evaluate the performance of FETs, the on-current I_{ON}, sub-threshold swing S_{s}, NW trap density $\mathrm{N_{trap}}$, and device mobility μ are calculated for all the fabricated devices. Fig. S9 presents the graphical estimation of the sub-threshold swing S_{s}, on/off current ($I_{\mathrm{ON/OFF}}$) and transconductance g_{m} using the LC FET measurement data of ACMAN Device 3 as shown in Fig. 4 (a) (Fig. S6(a)).

The S_{s} (V/dec) value describes the amount of gate voltage required to increase drain current by one order of magnitude in the sub-threshold region. The transfer characteristics of the Si NW FETs in logarithmic scale are used for the extraction of S_{s} values as shown in Equation (S8). The smaller S_{s} values, the quicker or sharper increasing of drain current. This sub-threshold behavior also indicates the difference in defect/trap states in the NWs or at the NW/dielectric interface. A higher density of traps results in a less steep current increase, as more trap states need to be filled. In other words, the value of $\mathrm{N_{trap}}$ expresses the level of defects. Equation (S9) shows the relationship between the traps density (N_{trap}) and the sub-threshold swing (S_{s}).

$$S_s = \frac{\Delta V_{\mathrm{G}}}{\Delta \log I_{\mathrm{DS}}}, \tag{S8}$$

and

$$N_{\mathrm{trap}} = \left[\frac{qS_s \log(e)}{kT} - 1\right] \frac{C_{\mathrm{NW}}}{2\pi n r L_{\mathrm{d}} q}, \tag{S9}$$

where V_{G} is the gate voltage, I_{DS} is the drain current, q is the elementary charge, k is the Boltzmann's constant, T is absolute temperature,

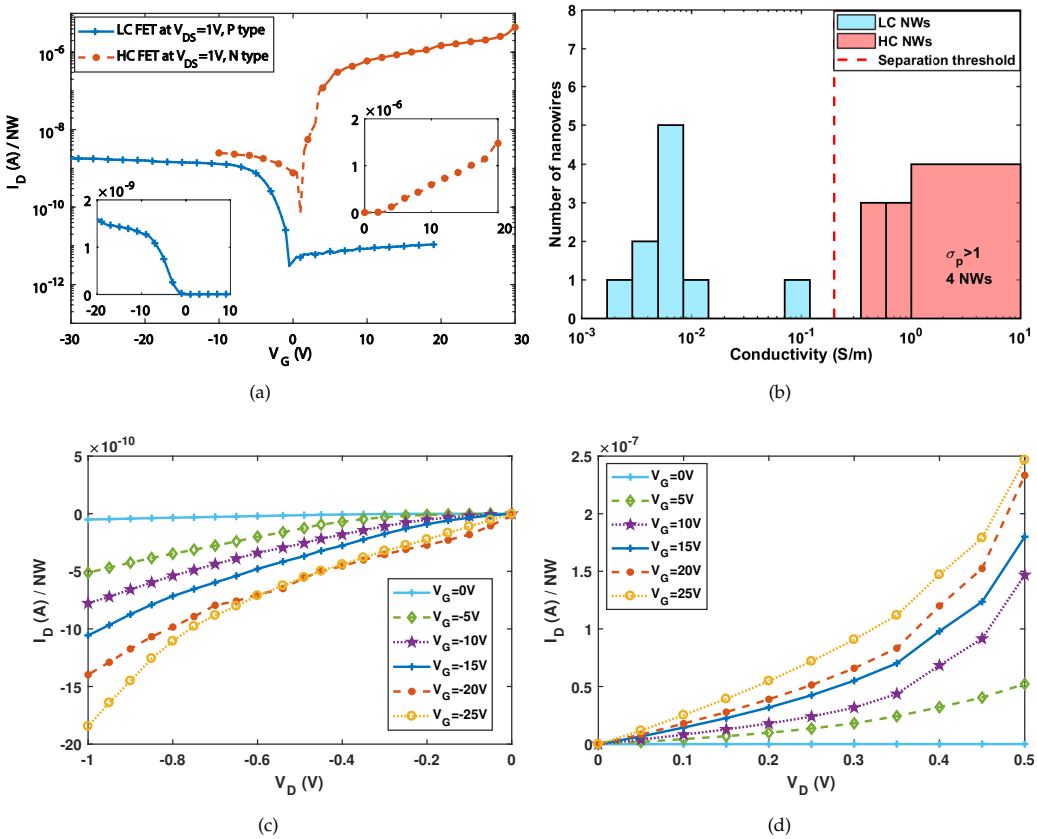


Fig. S6. ACMAN Device 3: A proof-of-concept demonstration of the integrated ACMAN process to separate and assemble Si NWs as FET devices. A total of 20 Si NWs were initially deposited, with 10 NWs selected and positioned on the HC and the LC sides, respectively, according to their conductivities using ACMAN. After the wrap-around electrode fabrication, the resulting FETs have 3 NWs on each side. The FET assembled with LC Si NWs shows p-type characteristics while the FET assembled with HC Si NWs shows n-type characteristics. (a) Transfer characteristics in logarithmic scale showing the drain current per nanowire at $V_{\mathrm{DS}} = 1$ V for the p-type and n-type FETs after separation. Inset: The transfer characteristics in linear scale. (b) Measured electrical conductivity distribution against the number of characterized nanowires by EOS characterization. (c) Output characteristics of the LC FETs showing the drain current per nanowire at $V_{\mathrm{G}} = 0$ to -25 V in -5 V steps. (d) Output characteristics of the HC FETs showing the drain current per nanowire at $V_{\mathrm{G}} = 0$ to 25 V in 5 V steps.

n is the total number of NWs across the channel gap, r is the NW radius (varying from 25 - 150 nm [6]), L_{d} is the channel gap width (15 μm), and C_{NW} is the total gate capacitance.

The mobility and gate capacitance are calculated respectively as

$$\mu = \frac{L_{\mathrm{d}}^2 g_{\mathrm{m}}}{C_{\mathrm{NW}} V_{\mathrm{SD}}}, \tag{S10}$$

where

$$C_{\mathrm{NW}} = \frac{2\pi\varepsilon_0\varepsilon_{\mathrm{pary}} L_{\mathrm{d}} n}{\cosh^{-1}\left(\frac{r+d}{r}\right)}, \tag{S11}$$

and ε_0 is the absolute permittivity, $\varepsilon_{\mathrm{pary}}$ is the dielectric constant of parylene C (3.15) and d is the thickness of the gate dielectric layer (600 nm). The transconductance $g_{\mathrm{m}} = \frac{\partial I_{\mathrm{DS}}}{\partial V_{\mathrm{G}}}$ is found by using the transfer characteristics of the Si NW FETs in linear scale.

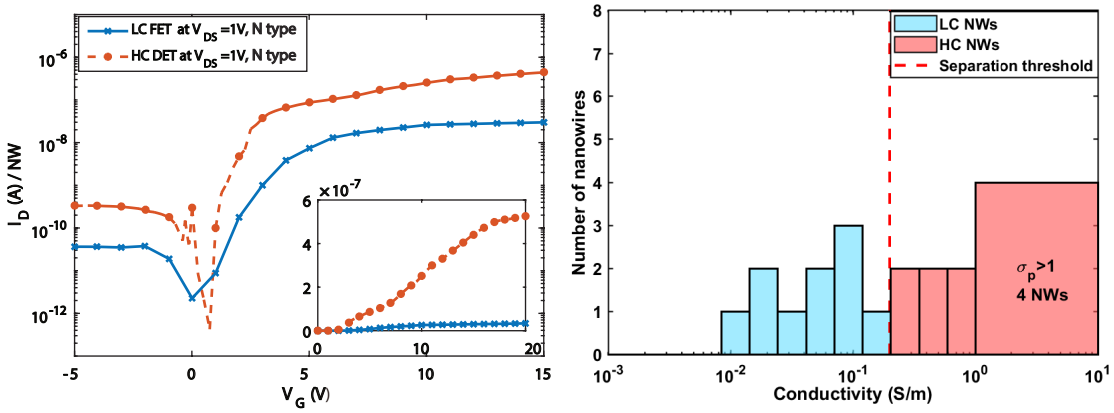
Table S1 summarizes the performance comparison of the FETs fabricated using the ACMAN scheme (ACMAN Devices 1 to 4) and DEP-only method (DEP-only Devices 1 to 4). In the table, HC stands for the FETs that are assembled by the selected more-conductive nanowires, and LC represents the FETs that are fabricated using the separated less-conductive nanowires. $R_{\mathrm{H/L}}$ denotes the ratio of the HC FET characteristics to the LC FET characteristics.

Supplementary figures

- Fig. S10 shows SEM image of as-grown silicon nanowires used in experiments.
- Fig. S11 shows the corresponding alignment rates measurement and crossover frequencies extraction shown in Fig. 3 and Supporting Movie 2.

Table S1. Performance comparisons for the FETs fabricated using the ACMAN process and DEP-only methods. The parameters are normalized to the number of NWs across the FET channel, thus showing an average current per NW.

		I_{on}/NW(A)	S_s(V/dec)	$N_{trap}(m^{-2})$	μ (cm^2/Vs)	NW No.	Type
ACMAN Device 1	HC	1.3×10^{-7}	1.43	2.8×10^{16}	$9.9 \pm 2.2 \times 10^{-1}$	10	N
	LC	1.3×10^{-9}	4.38	8.7×10^{16}	$6.2 \pm 1.4 \times 10^{-3}$	10	N
	$R_{H/L}$	100	33%	0.32	~ 160	1	same
ACMAN Device 2	HC	4.9×10^{-8}	2.16	4.3×10^{16}	4.4 ± 1.6	3	N
	LC	3.7×10^{-9}	-5.19	-1.0×10^{17}	$-1.2 \pm 0.6 \times 10^{-1}$	3	P
ACMAN Device 3	HC	4.4×10^{-6}	0.31	5.8×10^{15}	$4.7 \pm 1.1 \times 10$	3	N
	LC	1.8×10^{-9}	-0.62	-1.3×10^{16}	$-1.2 \pm 0.3 \times 10^{-1}$	3	P
ACMAN Device 4	HC	9.3×10^{-7}	0.11	1.6×10^{15}	9.0 ± 2.0	7	N
	LC	3.2×10^{-8}	0.70	1.3×10^{16}	$7.5 \pm 1.7 \times 10^{-1}$	9	N
	$R_{H/L}$	29	16%	0.12	~ 12	0.78	same
DEP-only Device 1	HC	1.0×10^{-7}	-2.47	-5.0×10^{16}	$-3.2 \pm 0.7 \times 10^{-1}$	2	P
	LC	2.6×10^{-8}	-10.10	-2.0×10^{17}	$-8.1 \pm 1.9 \times 10^{-1}$	3	P
	$R_{H/L}$	3.8	24%	0.25	~ 0.40	0.67	same
DEP-only Device 2	HC	5.0×10^{-10}	-7.90	-1.6×10^{17}	$-2.0 \pm 0.5 \times 10^{-4}$	12	P
	LC	5.2×10^{-11}	-2.19	-4.5×10^{16}	$-8.9 \pm 1.7 \times 10^{-4}$	50	P
	$R_{H/L}$	9.6	128%	3.56	~ 0.22	0.28	same
DEP-only Device 3	HC	2.5×10^{-11}	-1.90	-4.0×10^{16}	$-2.0 \pm 0.5 \times 10^{-4}$	7	P
	LC	1.5×10^{-11}	-2.18	-4.4×10^{16}	$-7.2 \pm 1.7 \times 10^{-5}$	42	P
	$R_{H/L}$	1.7	87%	0.91	~ 2.8	0.17	same
DEP-only Device 4	HC	2.57×10^{-7}	11.3	2.3×10^{17}	$-3.0 \pm 0.7 \times 10^{-1}$	7	N
	LC	8.2×10^{-8}	-2.96	-6.0×10^{16}	$-7.9 \pm 2.0 \times 10^{-2}$	43	P



(a) (b)

Fig. S7. ACMAN Device 4: A proof-of-concept demonstration of the integrated ACMAN process to separate and assemble FET devices with 20 Si NWs. A total of 20 Si NWs was initially deposited, with 10 NWs selected and positioned on the HC and the LC sides, respectively, according to their conductivities using ACMAN. After the wrap-around electrode fabrication, 9 NWs remain on the LC-side FET, and the HC-side FET has 7 NWs left, both showing n-type characteristics. (a) Transfer characteristics in logarithmic scale showing the drain current per nanowire at $V_{\mathrm{DS}} = 1$ V for the two n-type FETs after separation. Inset: The transfer characteristics in linear scale. (b) Measured electrical conductivity distribution against the number of characterized nanowires by EOS.

Media

- Supporting Movie 1: Design schematic of the ACMAN process for nanowire FET fabrication.
- Supporting Movie 2: Experimental video of characterizing and separating two silicon nanowires using the ACMAN scheme.

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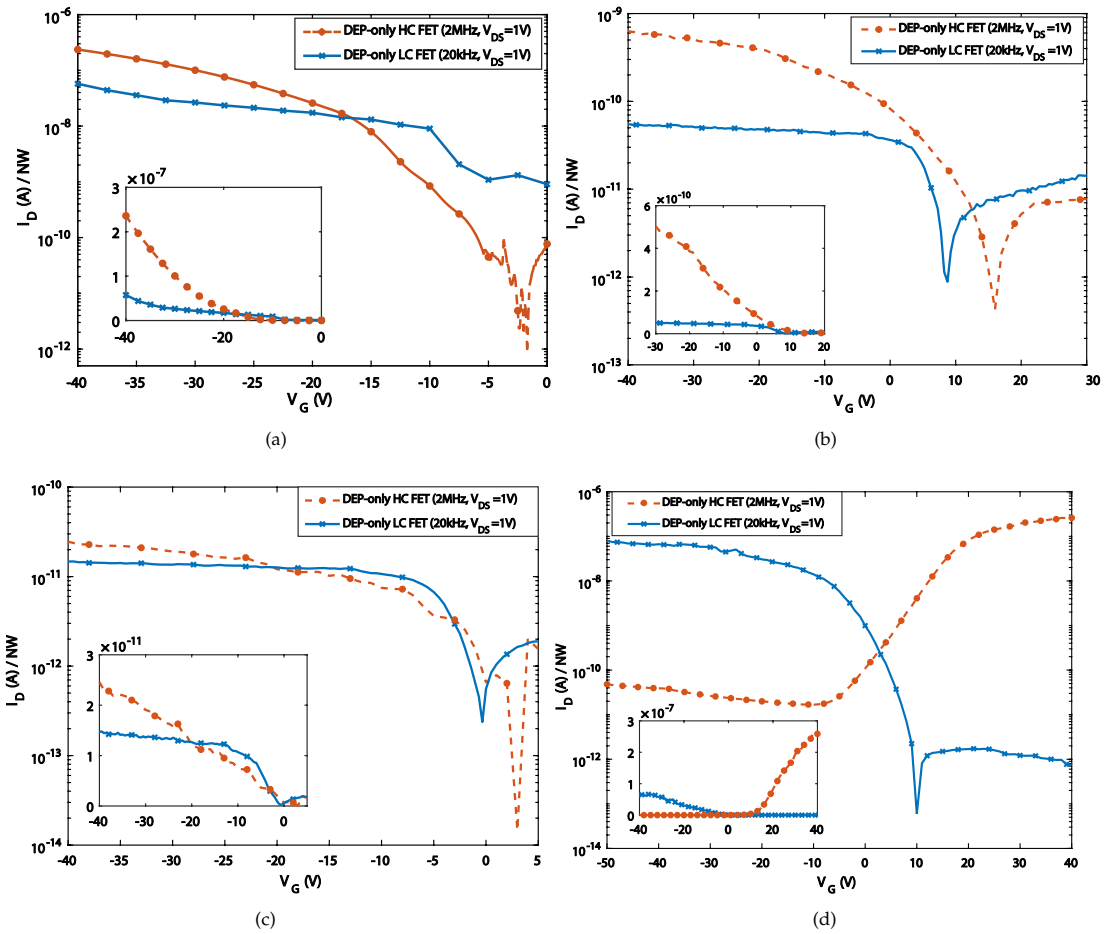

Fig. S8. Transfer characteristics of the DEP-only devices: Si NWs were collected at different DEP frequencies. 2 MHz and 20 kHz frequencies and 50 V_{pp} AC fields were used to fabricate the HC and the LC FETs, respectively. These frequencies are the same as used in the deposition step to trap nanowires for ACMAN Devices.

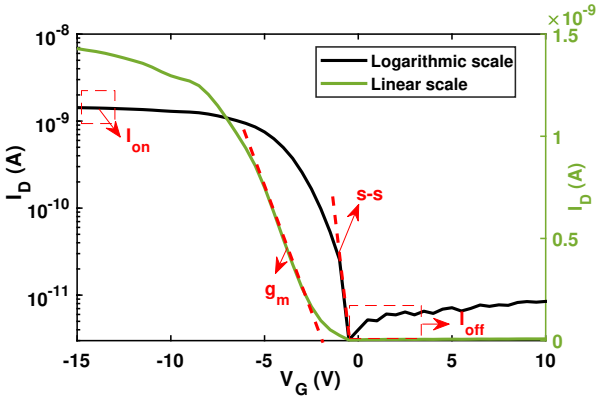

Fig. S9. Graphical presentation of the sub-threshold swing (S_s), on/off current ($I_{ON/OFF}$) and transconductance g_m using the LC FET measurement data of ACMAN Device 3 as shown in Fig. 4 (a).

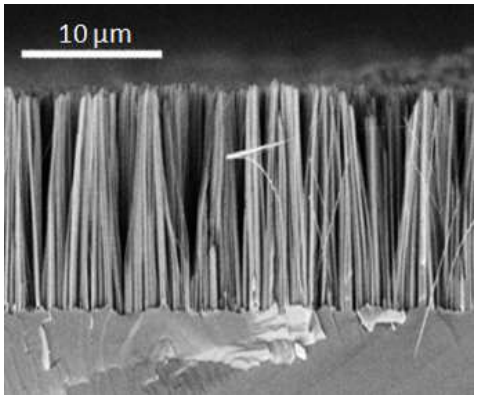

Fig. S10. SEM image of as-grown silicon nanowires used in experiments.

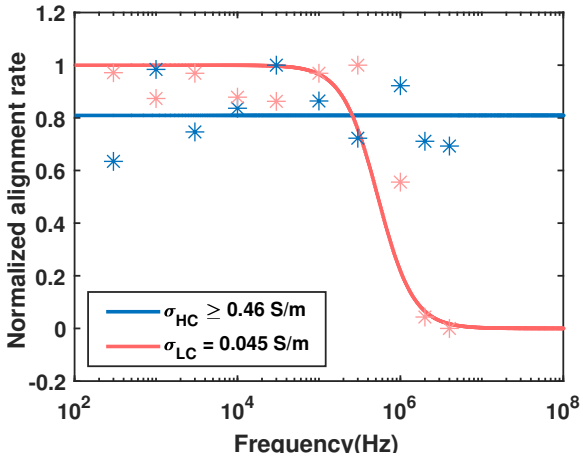

Fig. S11. Measured alignment rates of two simultaneous Si NWs in Fig. 3 with respect to the applied electric field frequencies. The solid lines are curve fit of the form $\Omega = 1/[1 + (\omega/\omega_c)^2]$, from which the crossover frequency and hence the nanowire electrical conductivity can be extracted.