Directed self-assembly of high-chi block copolymer for fabrication of optical nanoresonator

Sozaraj Rasappa[1*], Lars Schulte[2, 3], Sokol Ndoni[2, 3], Tapio Niemi[1*]

[1]Laboratory of Photonics, Tampere University of Technology, P. O. Box 692, FI-33101, Finland

[2]Department of Micro and Nanotechnology, Technical University of Denmark, DK-2800 Kgs, Lyngby, Denmark

[3]Center for Nanostructured Graphene, Technical University of Denmark, DK-2800 Kgs, Lyngby, Denmark

[*]Corresponding authors: sozaraj.rasappa@tut.fi, tapio.k.niemi@tut.fi

Supporting information

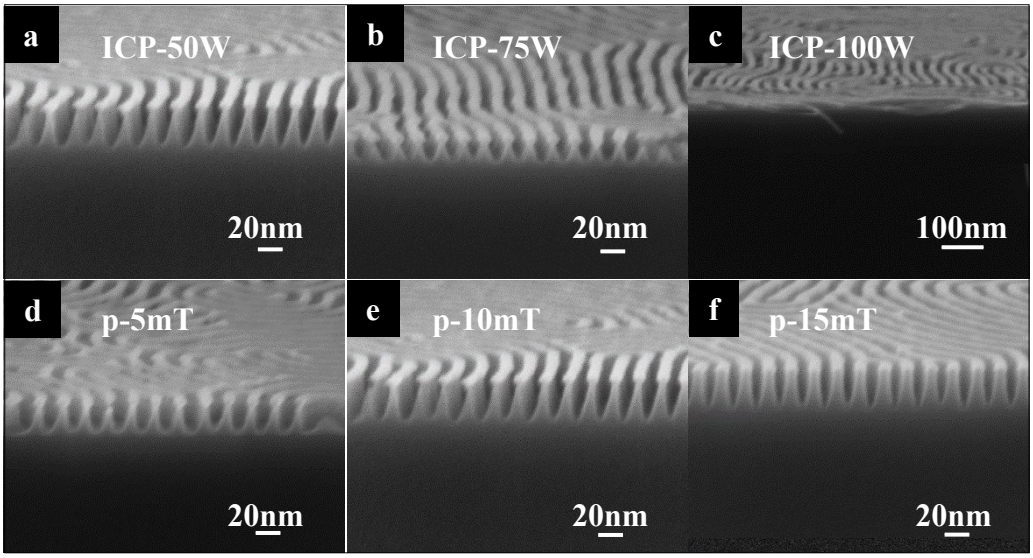


Figure SI1: Optimisation of Si etch parameter using Cr hard mask. (**a–c**) Varying ICP power. (**d–f**) Varying chamber pressure.

Figure SI1a–f shows the etch optimisation of the underlying Si, using the Cr nanolines as the etch mask. For this study, the etch parameters, such as gas flow rates and time, are kept constant at SF_6 = 50 sccm, O_2 = 40 sccm, RIE = 30 W and t = 18 s. The high O_2 gas flow level helps passivate the sidewall for achieving a deep etch. The increase in ICP power from

50 to 100 W leads to more isotropic etch and the risk of losing the sidewall-controlled Si etch, as shown in Figure SI1a–c. Figure 2c clearly reveals that a severe undercut has been developed at 100 W ICP power without affecting the Cr mask. The pressure in the etch chamber also makes a huge impact on the etch depth, as shown in Figure SI1d–e. The increase in pressure increases the Si etch depth, and the PDMS mask on top of the Cr lines vanishes at 50 W ICP for the etch time of t = 18 s, as shown in Figure SI1f, and leaves only Cr lines. Figure 1e in the main text shows the Si nanofin structures fabricated by using the Cr mask and the optimised etch parameters, as follows: SF_6 = 50 sccm, O_2 = 40 sccm, p = 15 mT, ICP = 50 W, RIE = 30 W and t = 54 s.

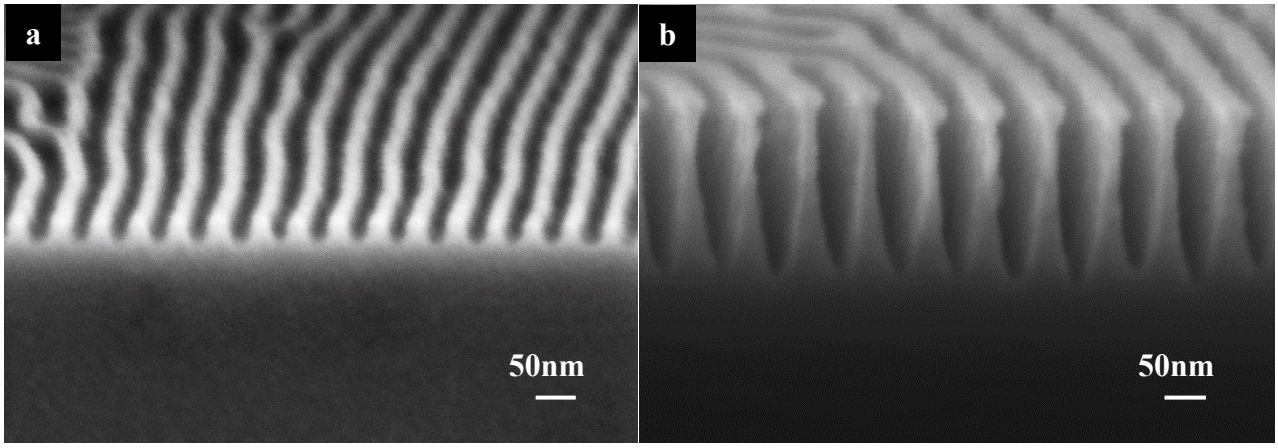


Figure SI2. Cross-sectional SEM images of Si nanostructures. (**a**) Si nanolines after pattern transfer using oxidised PDMS mask. (**b**) Si nanofins after pattern transfer using Cr hard mask.

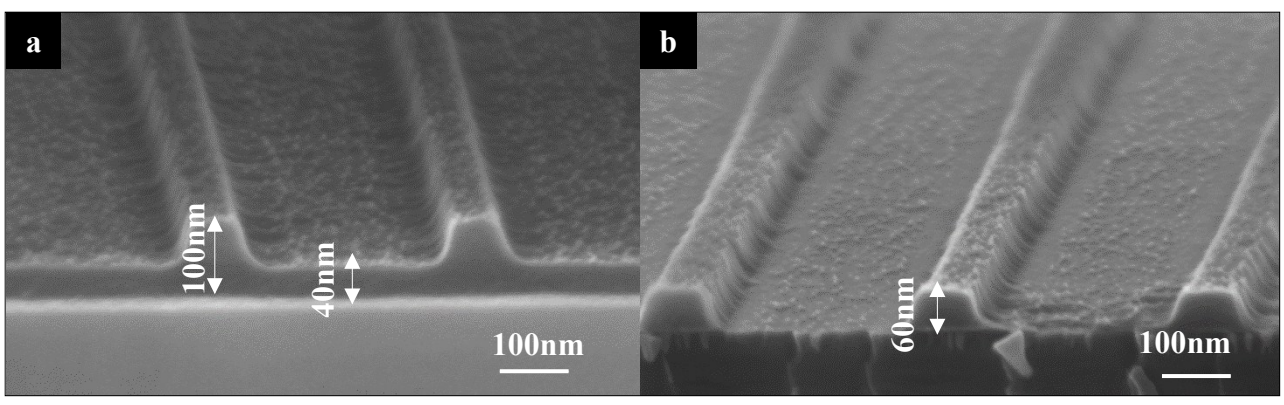
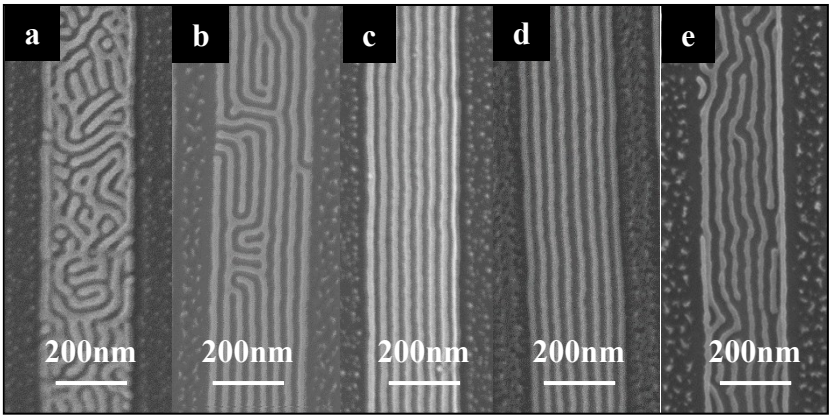


Figure SI3. NIL template fabrication. (**a**) Cross-sectional SEM image after NIL imprint. (**b**) Cross-sectional SEM image after residual layer removal.

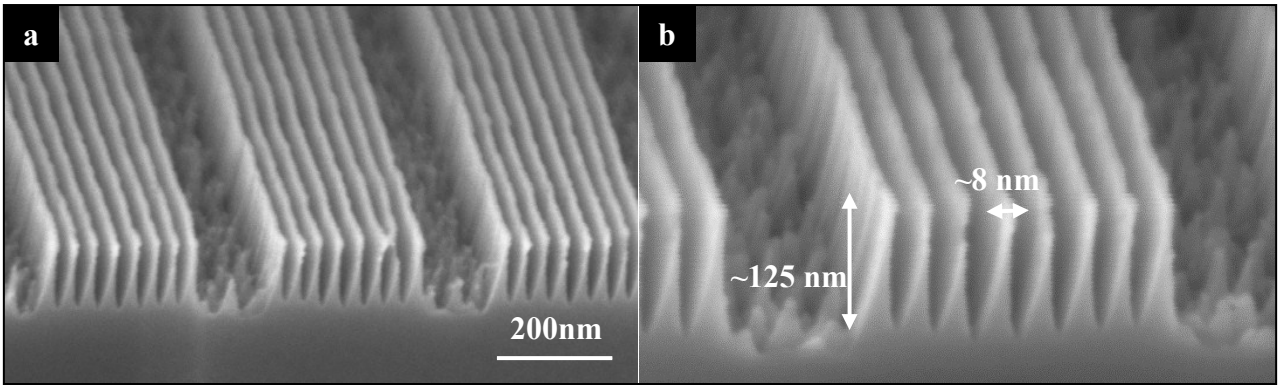
The UV-based NIL was used to fabricate Si trench substrates. The NIL stamp, with a trench width of ~300 nm and a mesa width of ~100 nm, was imprinted on a UV-curable NIL resist. The NIL template on the Si substrate after the imprint with a 100-nm height and the residual resist layer, is shown in Figure SI3a. The residual resist was removed by using O_2 plasma,



while the initial template height of 100 nm was reduced to ~60 nm, as shown in Figure SI3b.

Figure SI4. Top-down SEM image of PDMS lines after Cr etch. (**a–d**) SD thin film annealed for 0, 15, 30 and 45 min, respectively, on Cr-coated NIL substrate. (**e**) SD thin film annealed for 30 min on NIL substrate without Cr layer.

SD thin films were annealed for 0 to 45 min to induce the DSA on Cr-coated NIL patterned SOI substrates, as shown in Figure 4a–d. The long-range parallel alignment was achieved after 30 min of annealing time under toluene vapour, as shown in Figure 4c–d. The optimised DSA annealing conditions were applied on the NIL substrate without the Cr layer, as shown in Figure 4e. This clearly shows that the O_2 plasma that is used to remove the residual NIL resist layer



tunes the surface of Si and produces defects in the SD self-assembly. Hence, the Cr coating is not only useful as a hard mask but also improves the surface quality for templating.

Figure SI5. Cross-sectional SEM images of Si nanofins. (**a**) Si nanofins after Cr mask removal. (**b**) High magnification SEM image of Si nanofins.

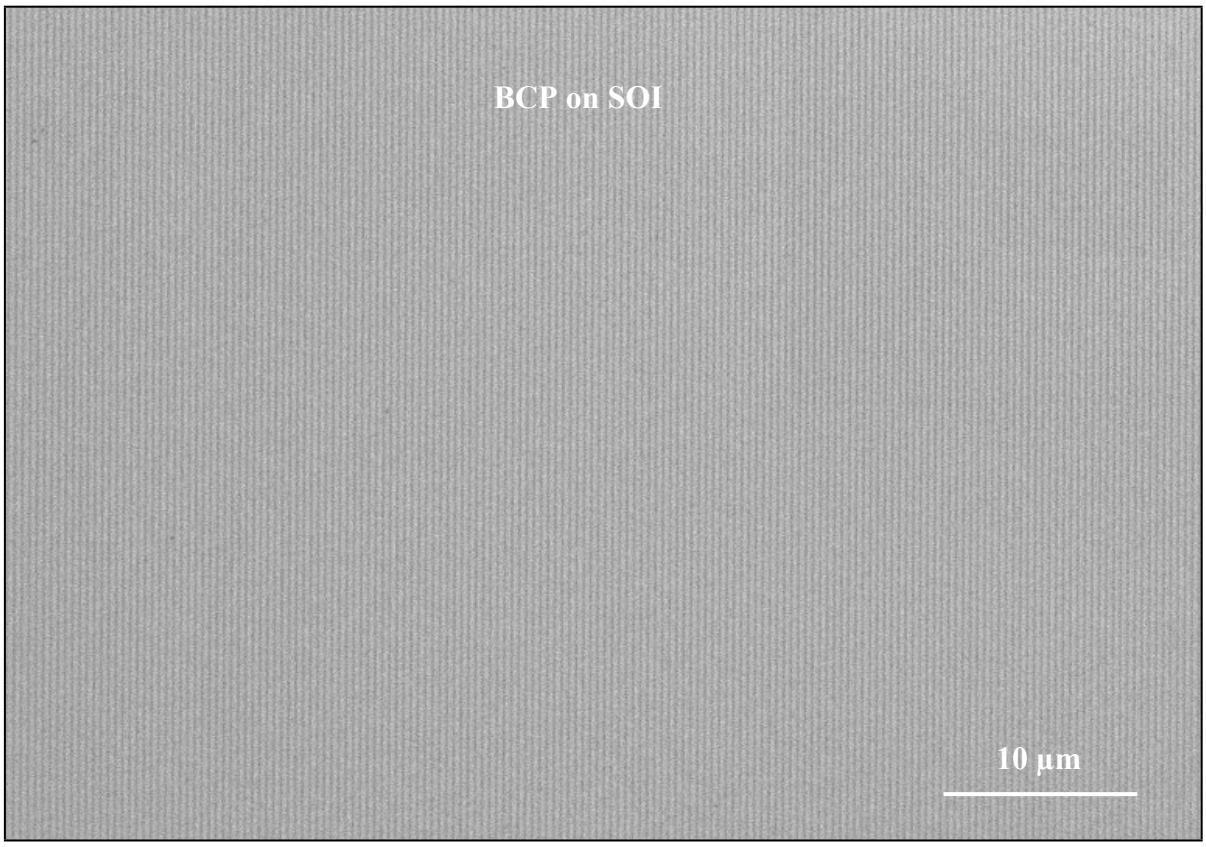


Figure SI6. Large-scale SEM image of DSA on SOI substrate.

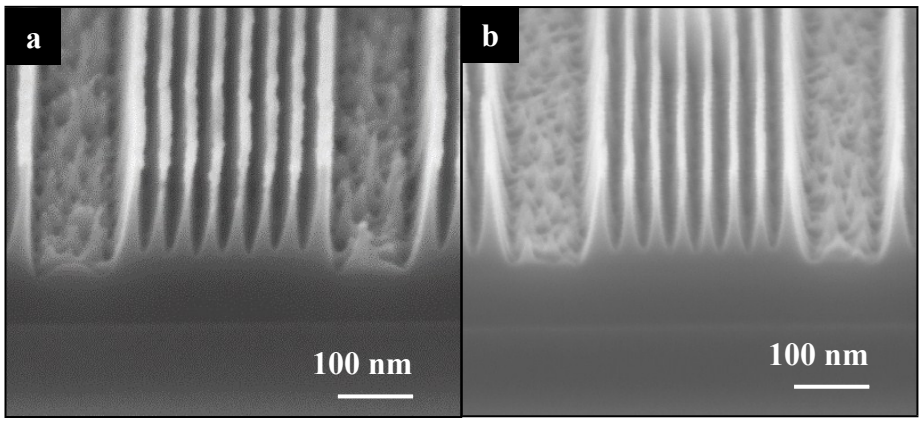


Figure SI7. Cross-sectional SEM images of SOI nanofins. (**a**) SOI nanofins with Cr mask. (**b**) SOI nanofins without Cr mask.

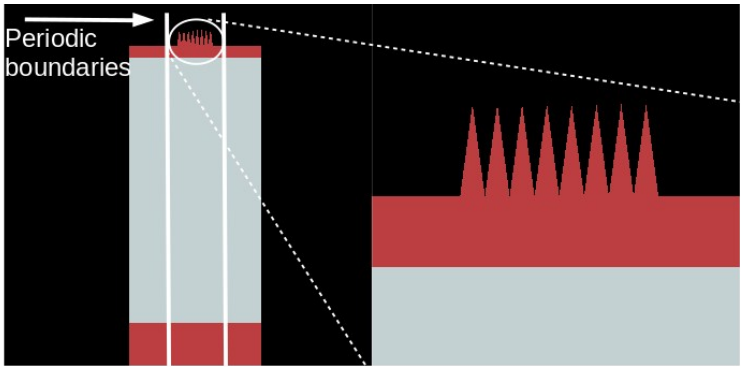


Figure SI8. Simulation setup for the nanostructured GMR waveguide.

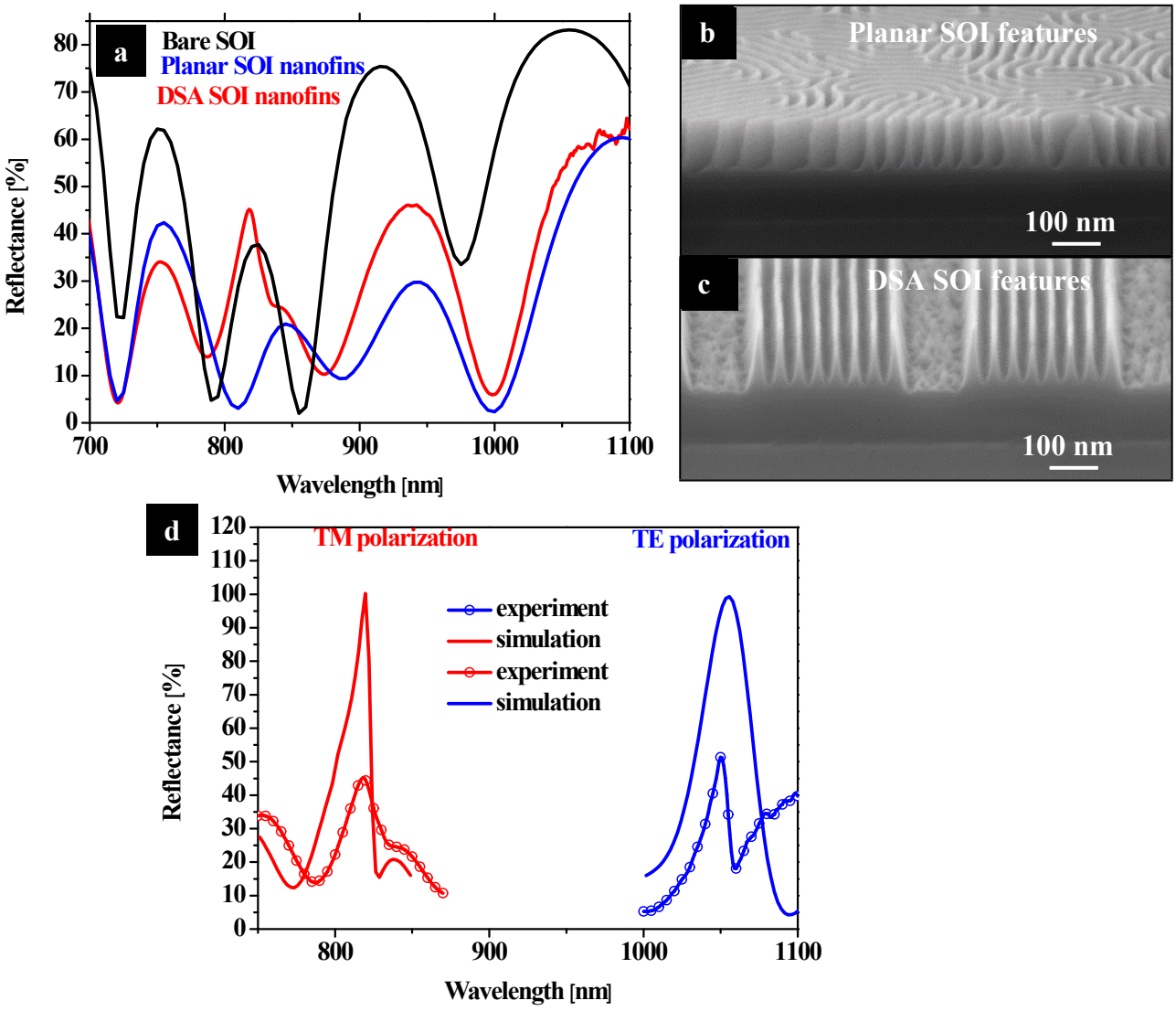


Figure SI9. Reflectance measurements and SEM images. (**a**) Measured reflectance of bare SOI, nanofins on plain SOI and nanofins by DSA on SOI. (**b**) SOI ridges on planar substrate. (**c**) SOI ridges on DSA substrate. (**d**) Comparison of measurements and simulations.