Supplementary Materials for Beyond SiO$_x$: An Active Electronics Resurgence and Biomimetic Reactive Oxygen Species Production and Regulation from Mitochondrion

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Figure S1: TEM image of MIS-edge device.

Figure S2: SEM images (top image: top view; bottom image: side view) of the nm-scale device by Nanosphere Lithography.
Figure S2 shows the nm-scale dimension of SiO$_x$-based resistive switching elements with scanning electron microscope images (Zeiss Neon 40 SEM) (top image: top view of devices; bottom image: side view of devices). The detailed procedure of SiO$_x$-based resistive switching elements fabrication begins with e-beam evaporation (PVD, CHA Industries) of 60 nm of SiO$_x$ (measured by ellipsometer) on a N$^{++}$ (100) Si substrate ($1-7 \times 10^{19}$ cm$^{-3}$, the resistivity of 0.001–0.005 ohm-cm) used as a bottom electrode. Next, the PVD-SiO$_x$ layer is treated in an oxygen plasma reactor to obtain a hydrophilic surface. 18 M$\Omega$ DI water and 200 nm polystyrene nanospheres (Polysciences, Inc.) were used for nanosphere mask preparation. The 200 nm nanosphere was chosen due to a trade-off between minimum feature size and larger-scale uniformity. Polystyrene nanosphere solution was dropped on top of microscope coverslips. This was then introduced to the air-water interface in a Petri dish filled with 18M$\Omega$ DI water. The polystyrene solution spreads out at the air-water interface forming a monolayer. Prior to monolayer formation, a prepared silicon substrate with SiO$_x$ coating was immersed at the bottom of a Petri dish. The monolayer was then transferred to an immersed substrate by slightly lifting the substrate. Then the sample was dried in air. The diameter of each NS in the monolayer was reduced by reactive ion etching (Oxford 80 RIE) in oxygen-plasma (80 sccm O$_2$; power 60 W; pressure 100 mT; 3 min). The power, partial pressure, and time of etching were optimized to obtain the desired size. The resistive switching elements are formed by RIE (5 sccm Ar + 5 sccm O$_2$ + 80 sccm CF$_4$; power 100 W; pressure: 200 mT) to transfer the treated NS pattern into the SiO$_x$ layer. On the basis of the resistive switching elements, nanopillars are obtained via Bosch deep silicon etch process (Versaline Deep Silicon Etch System, Plasma-Therm Inc.). The NS layer was removed by bath sonication in water for 15 min.
Figure S3: 540*540 µm$^2$ Device. Lorentzian Fitting functions and parameters: area, full width at half maximum (FWHM), L: amplitude. $\Gamma$: FWHM. $X_o$: Center. Formula:

$$L(x) = \frac{\pi}{\frac{1}{2}\Gamma} \frac{1}{(x-x_o)^2 + \left(\frac{1}{2}\Gamma\right)^2}.$$ 

The rainbow-colored lines in each figure are the sub-fitting peaks; black line (almost overlap with raw data points) is the final fitting results for area estimation.
Figure S4: 50*50 nm^2 Lorentzian fitting results. The rainbow-colored lines in each figure are the sub-fitting peaks; black line (almost overlap with raw data points) is the final fitting results for area estimation.
Figure S5: Static and dynamic bandgap modeling: a proton exchange reaction in SiO$_x$. 
Figure S5: **Static and dynamic** Energy band diagrams showing theoretical bandgaps of Si-H-Si and SiH+SiSi(5), 2.5 eV offset of H$_3$O$^+$ energy level from Si-H-Si conduction band, switching
region of length and Fowler-Nordheim tunneling RESET transition (Figure S5 (a-b),[58, 60, 62, 68] and Figure S5 (e) with voltage increasing on top panel); and HRS showing theoretical bandgap of (SiH)$_2$ defect within gap region of length and trap-assisted tunneling SET transition (Figure S5 (c-d),[58, 60, 62, 68] and Figure S5 (e) with voltage increasing on bottom panel).

Figure S6: Threshold switching in the air (A-TS) for selectivity and nonlinearity calculation.

![Graph showing selectivity (a.u.) vs. Half-Read Voltage (V)](image)

Figure S7: TEM images and EDX results at the interface of SiO$_x$ and SiO$_x$/3nm-HfO$_x$ devices.
Figure S8: Pre-processing of the ROS-like signals to training information

1. Remove P-F background current and keep the ROS-like signals (by S3 and S4).
2. Mapping the sequential order of voltage range (from 3V to 8V) with amplitude on 16*16 (256 bits) array as training neurons. For example, setup column 0-row 0 as voltage 3, increase from column number (from 0 to 15) at fixed row number with voltage increasing from 3V to 3.29V, then following increase with row number (from 0 to 15) and sequential column number increasing, for example, column 0-15 at fixed row number (#1) by 3.31V to 3.61.

3. Topology patterns (TPs) as a function of ambient effect.

![Figure S9](image)

*Figure S9: Optimization simulation results for the best training and learning process: The characteristics of different LTP and LTD working as a pattern recognition network.*