Supporting information

Polarity-controllable MoS$_2$ transistor for adjustable complementary logic inverter application

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Fig. S1: Material characterization of the double gate MoS$_2$ FET (a) Raman spectrum (b) PL spectrum and (c) TEM image, indicating the uniformity is smooth with thickness around 5nm in multilayer formation (the peak difference between A$_{1g}$ and E$_{2g}$ is 25 cm$^{-1}$ whereas PL signal is relatively weak).

Fig. S2: The I$_d$-V$_g$ characteristic of the double gate MoS$_2$ FET with the operation of top gate voltage at different values of V$_d$. 
Fig. S3: The other device top gate with SiO$_2$ layer shows transfer characteristics with both PMOS and NMOS behavior while the operation of (Left) the top gate and (Right) the back gate voltage.

Fig. S4: The $I_{gs}$-$V_g$ curves of the proposed device, showing the common leakage current of a few pA.
Fig. S5: The $I_d-V_g$ curves of the proposed device in the operation of the back gate before and after top gate process, indicating that the channel has been damaged after depositing dielectric materials instead of poor contact affecting the mobility and current density.
**Border traps mechanism**

Capture/emission is the primary method of interaction between the electrons/holes in the substrate and the interface traps; while tunneling is the primary transport method of electrons/holes from the semiconductor interface to the border trap and back. Fig. S6(a) shows the flat band diagram indicating the interface and border traps occupied by electrons up to the Fermi level $E_F$.

When a positive bias is applied as in Fig. S6(b), interface traps capture electrons from the conduction band and then these inversion electrons tunnel from the interface towards the lower energy border traps until a level equal to $E_F$ is occupied. As a result, the oxide presents negative charges. On the other hand, when a negative bias is applied as in Fig. S6(c), the result is reversed. Here, electrons tunnel from border traps to the conduction band, interface traps and the valence band. Hence, the electrons that compensate positively charged defects leave the oxide [1,2].

**Fig. S6:** Schematic plot of the border traps and interface traps mechanism model. [1]
Fig. S7: The (Left) voltage transfer characteristics of another CMOS inverter as a function of \( V_d \) and the (Right) corresponding \( I_d-V_g \) characteristic of the top gate and back gate structure at \( V_d = 1.1 \) V.

Fig. S8: The \( I_d-V_g \) characteristics of the other top gate structure as a function of gate voltage pulse duration (\( T_{GS} \)), and the corresponding current density and \( V_{th} \) tendency at different values of \( T_{GS} \).
Fig. S9: (Left) The voltage transfer characteristics of the other CMOS inverter at $V_d$ equal to 2.1 V. The black curve and red curve are the results before and after applying the gate voltage pulse ($T_{GS}$). (Right) The corresponding gain characteristics of the CMOS inverter at $V_d$ equal to 2.1 V.

<table>
<thead>
<tr>
<th>Pulse duration</th>
<th>Pristine</th>
<th>1s</th>
<th>2s</th>
<th>3s</th>
</tr>
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<tbody>
<tr>
<td>Current density (A) at -6V</td>
<td>$1.22 \times 10^{-7}$</td>
<td>$1.69 \times 10^{-7}$</td>
<td>$2.7 \times 10^{-7}$</td>
<td>$4.55 \times 10^{-7}$</td>
</tr>
<tr>
<td>Threshold voltage ($V_{th}$)</td>
<td>-3.55V</td>
<td>-2.7V</td>
<td>-2.15V</td>
<td>-1.6V</td>
</tr>
</tbody>
</table>

Table S1. The corresponding current density at -6V and $V_{th}$ values in a fixed gate voltage pulse of -8V at various duration times while gate voltage sweep from -8V to 8V.
The details of the corresponding theoretical calculations

The semiconductor potential, \( \phi_B \), is described by the relation below:

\[
\phi_B = V_t \ln \left( \frac{N_A}{n_i} \right) = 0.0259 \ln \left( \frac{10^{11}}{10^{10}} \right) = 0.059V
\]

and the maximum inversion width (\( X_{dT} \)) calculated below:

\[
X_{dT} = \frac{\pi \varepsilon_s (2\phi_B)}{\ln(4)eN_dT} = \frac{\pi \times 11 \times 8.85 \times 10^{-14} \times 2 \times 0.059}{\ln(4) \times 1.6 \times 10^{-19} \times \frac{10^{11}}{T} \times T} = 1.62 \times 10^{-5} \text{cm}
\]

where \( T \) is the semiconductor thickness.

The charge in the depletion region at strong inversion, \( |Q'_{SD(max)}| \), can then be determined using the formula:

\[
|Q'_{SD(max)}| = eN_dX_{dT} = 1.6 \times 10^{-19} \times \frac{10^{11}}{4 \times 10^{-9} \times 10^2} \times 1.62 \times 10^{-5} = 6.48 \times 10^{-7} \text{C/cm}^2
\]

When applying a positive gate bias during the back gate operation, the \( \phi_{ms} \) can be described by:

\[
\phi_{ms} = \phi' - \left( \frac{E_g}{2e} + \phi_B \right) = 4.25 - \left( 3.7 + \frac{1.4}{2} + 0.059 \right) = -0.209V
\]

The corresponding trapped oxide charges \( Q'_{ss} \) is calculated by the measured \( V_{th} \) of 6.4 V (Fig. 2(e)) through the \( V_{th} \) formula:

\[
V_{th} = \left( |Q'_{SD(max)}| - Q'_{ss} \right) \frac{\varepsilon_{ox}}{\varepsilon_{ox}} + \phi_{ms} + 2\phi_B
\]

\[
6.4 = \left( 6.48 \times 10^{-7} - Q'_{ss} \right) \left( \frac{30 \times 10^{-9} \times 10^2}{3.9 \times 8.85 \times 10^{-14}} \right) + (-0.209) + 2 \times 0.059
\]

\[
Q'_{ss} = \left( 6.48 \times 10^{-7} + \frac{-6.4 + (-0.209) + 2 \times 0.059}{30 \times 10^{-9} \times 10^2} \right) \left( \frac{3.9 \times 8.85 \times 10^{-14}}{3.9 \times 8.85 \times 10^{-14}} \right) = -9.87 \times 10^{-8} \text{C/cm}^2
\]

When applying a negative gate bias during the back gate operation, the \( \phi_{ms} \) can be described by:
\[ \varphi_{ms} = \varphi_m' \left( \chi' + \frac{E_g}{2e} - \varphi_B \right) = 4.25 - \left( 3.7 + \frac{1.4}{2} - 0.059 \right) = -0.091V \]

In order to meticulously fit our experimental results, we assume the \( \text{V}_{th} \) is -8 V in the ambipolar characteristic of the device. The \( \text{V}_{th} \) can be described by:

\[
\text{V}_{th} = \left( - |Q'_{SD(max)}| - Q'_{ss} \frac{t_{ox}}{E_{ox}} \right) + \varphi_{ms} - 2\varphi_B
\]

\[
-8 = \left( -6.48 \times 10^{-7} \right) \frac{30 \times 10^{-9} \times 10^2}{3.9 \times 8.85 \times 10^{-14}} + (-0.091) - 2 \times 0.059
\]

\[
Q'_{ss} = \left( -6.48 \times 10^{-7} + \frac{8 - 0.091 - 2 \times 0.059}{30 \times 10^{-9} \times 10^2} \right) = 2.48 \times 10^{-7} \text{C/cm}^2
\]

Basically, \( Q'_{ss} \) is composed of bias-dependent border traps-induced charges (\( Q_V \)) which border traps related descriptions are shown in SF3 and bias-independent oxide charges (\( Q_S \)) which include fixed oxide charges, mobile ionic charges, and oxide trapped charges to name a few. Due to the bias-dependence of \( Q_V \), the relationship of \( Q'_{ss} \) with \( Q_S \) and \( Q_V \) can be expressed using two different equations depending on the polarity of the applied gate bias. Using these equations,

\[
Q'_{ss} = \begin{cases} 
Q_S - Q_V = -9.87 \times 10^{-8} \text{cm}^{-2} \\
Q_S + Q_V = 2.48 \times 10^{-7} \text{cm}^{-2}
\end{cases}
\]

By solving simultaneous equations above, \( Q_V \) is found to be about \( 7.49 \times 10^{-8} \) C/cm\(^2\), while \( Q_S \) is about \( 3.46 \times 10^{-7} \) C/cm\(^2\).

For the top gate operation, we also considered the influence of border traps in calculating the top gate dielectric layers’ charges accordingly. When a positive bias is applied, the \( \varphi_{ms} \) can be described by:

\[ \varphi_{ms} = \varphi_m' \left( \chi' + \frac{E_g}{2e} + \varphi_B \right) = 4.5 - \left( 3.7 + \frac{1.4}{2} + 0.059 \right) = 0.041V \]

Note that electron affinity, \( \chi' \), in the SiO\(_2\)-MoS\(_2\) interface for the top gate structure is used for the
We also assumed the quantities $V\th$ while the measured $V\th$ was assumed to be 8 V.

\[
V\th = \left[ Q_{SD(max)} \left( \frac{t_{ox1}}{\epsilon_{ox1}} + \frac{t_{ox2}}{\epsilon_{ox2}} - Q_{ss1} \left( \frac{t_{ox1}}{\epsilon_{ox1}} - Q_{ss2} \left( \frac{t_{ox2}}{\epsilon_{ox2}} \right) \right) + \phi_{ms} + 2\phi_B \right] = 6.591V
\]

We assumed the quantities $V_V = Q_{V1}(t_{ox1}/\epsilon_{ox1}) + Q_{V2}(t_{ox2}/\epsilon_{ox2})$ and $V_S = Q_{S1}(t_{ox1}/\epsilon_{ox1}) + Q_{S2}(t_{ox2}/\epsilon_{ox2})$. Here, $V_V$ and $V_S$ are both contributed by the top gate structure’s HfO$_2$ ($Q_{V1}$ and $Q_{S1}$) and SiO$_2$ ($Q_{V2}$ and $Q_{S2}$) dielectric layers.

\[
\rightarrow -V_S + V_V = 6.591V
\]

Meanwhile, in the negative bias condition, the $\phi_{ms}$ can be described by:

\[
\phi_{ms} = \phi_m - \left( \chi + \frac{E_g}{2e} - \phi_B \right) = 4.5 - \left( 3.7 + \frac{1.4}{2} - 0.059 \right) = 0.159V
\]

\[
V_{th} = \left[ -Q_{SD(max)} \left( \frac{t_{ox1}}{\epsilon_{ox1}} + \frac{t_{ox2}}{\epsilon_{ox2}} - Q_{ss1} \left( \frac{t_{ox1}}{\epsilon_{ox1}} - Q_{ss2} \left( \frac{t_{ox2}}{\epsilon_{ox2}} \right) \right) + \phi_{ms} - 2\phi_B \right] = 3.697V
\]

We also assumed the quantities $V_V = Q_{V1}(t_{ox1}/\epsilon_{ox1}) + Q_{V2}(t_{ox2}/\epsilon_{ox2})$ and $V_S = Q_{S1}(t_{ox1}/\epsilon_{ox1}) + Q_{S2}(t_{ox2}/\epsilon_{ox2})$.

\[
\rightarrow -V_S - V_V = -3.697V
\]
\[ V_{total} = \begin{cases} 
-V_s + V_v = 6.591 V \\
-V_s - V_v = -3.697 V 
\end{cases} \]

By solving simultaneous equations above, we get \( V_v \) at 5.144V, and \( V_s \) equal to -1.447V.

References
