Electronic Supplementary Material (ESI) for Nanoscale Horizons.

Supporting information

Polarity-controllable MoS_2 transistor for adjustable complementary logic inverter application

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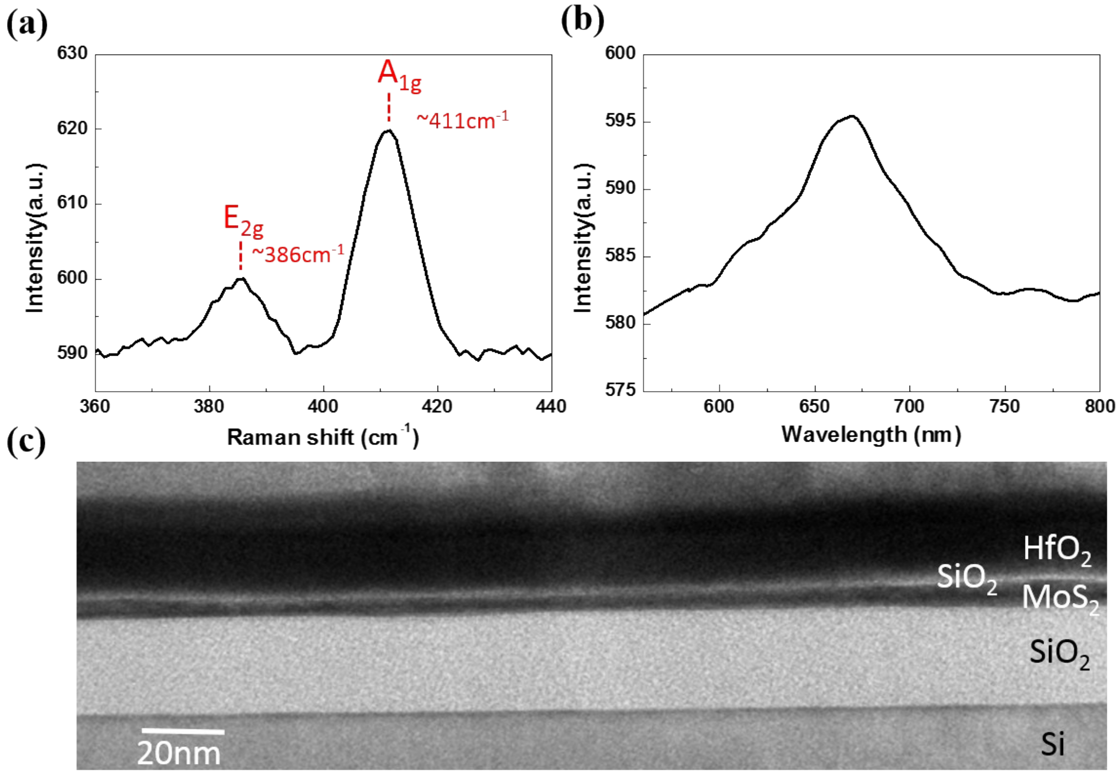

Fig. S1: Material characterization of the double gate MoS_2 FET (a)Raman spectrum (b)PL spectrum and (c)TEM image, indicating the uniformity is smooth with thickness around 5nm in multilayer formation (the peak difference between A_{1g} and E_{2g} is 25 cm^{-1} whereas PL signal is relatively weak).

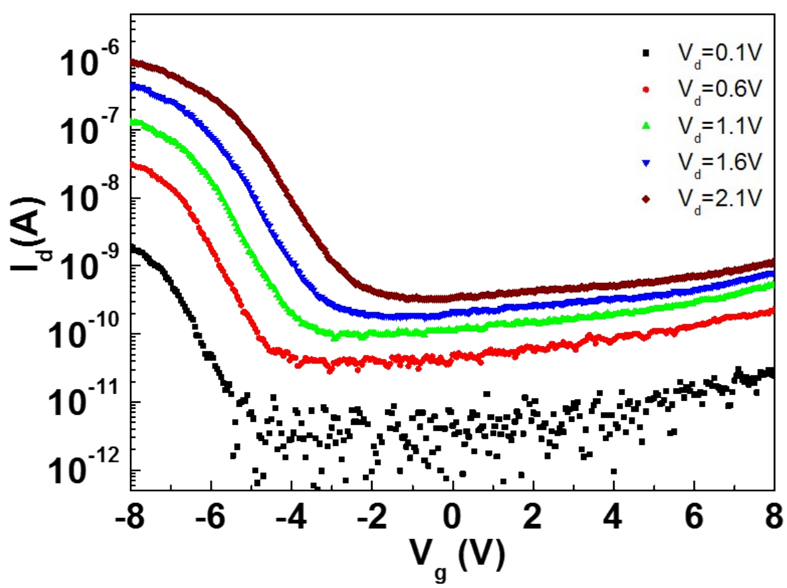

Fig. S2: The I_d-V_g characteristic of the double gate MoS_2 FET with the operation of top gate voltage at different values of V_d.

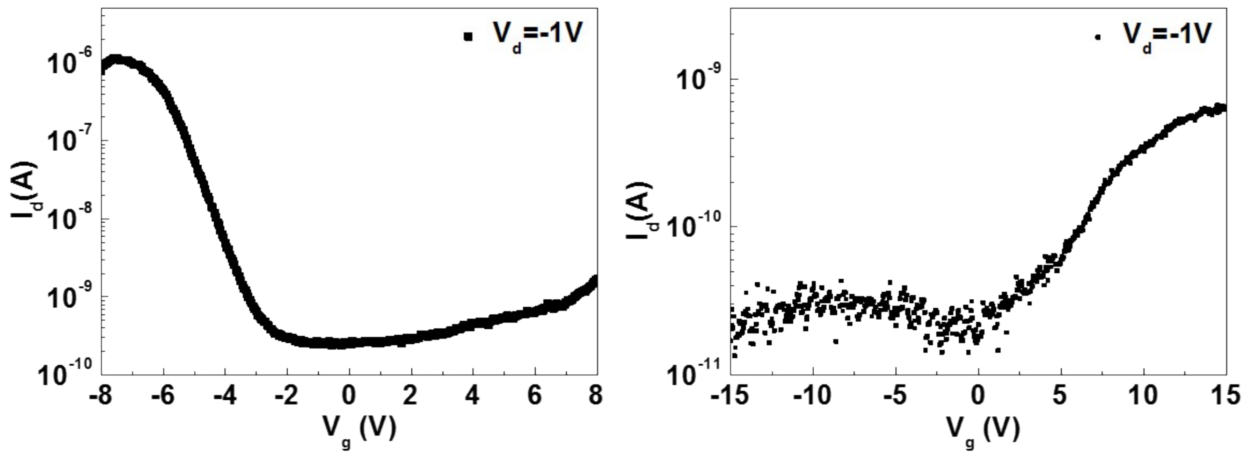

Fig. S3: The other device top gate with SiO_2 layer shows transfer characteristics with both PMOS and NMOS behavior while the operation of (Left) the top gate and (Right) the back gate voltage.

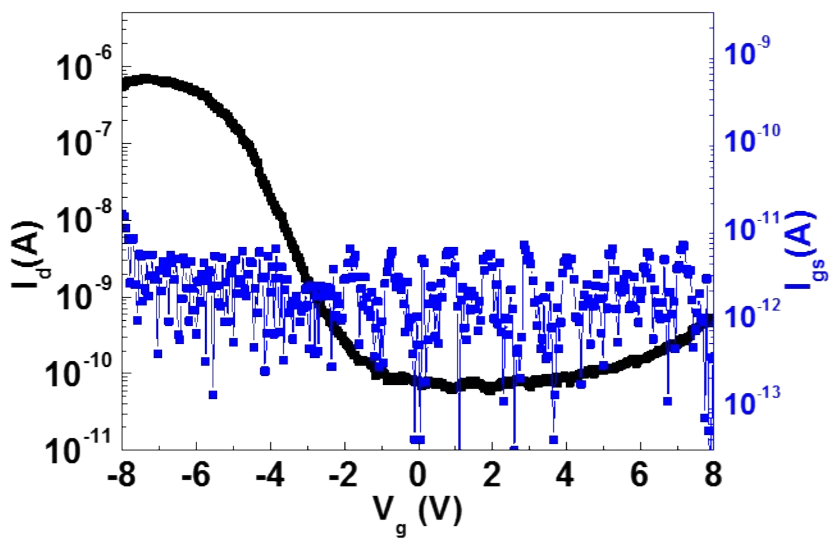

Fig. S4: The I_{gs}-V_g curves of the proposed device, showing the common leakage current of a few pA.

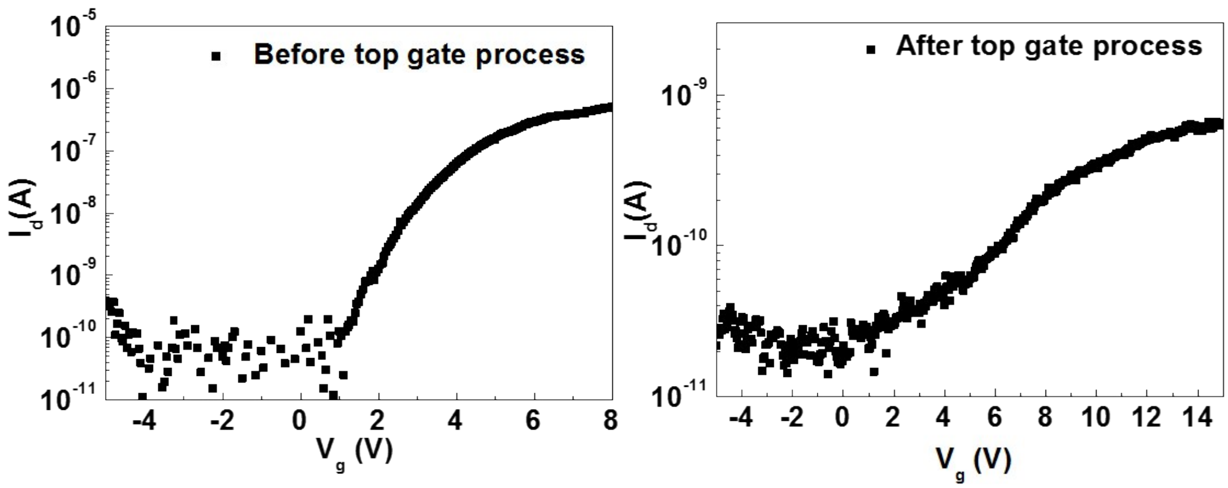

Fig. S5: The I_d-V_g curves of the proposed device in the operation of the back gate before and after top gate process, indicating that the channel has been damaged after depositing dielectric materials instead of poor contact affecting the mobility and current density.

Border traps mechanism

Capture/emission is the primary method of interaction between the electrons/holes in the substrate and the interface traps; while tunneling is the primary transport method of electrons/holes from the semiconductor interface to the border trap and back. Fig. S6(a) shows the flat band diagram indicating the interface and border traps occupied by electrons up to the Fermi level E_F.

When a positive bias is applied as in Fig. S6(b), interface traps capture electrons from the conduction band and then these inversion electrons tunnel from the interface towards the lower energy border traps until a level equal to E_F is occupied. As a result, the oxide presents negative charges. On the other hand, when a negative bias is applied as in Fig. S6(c), the result is reversed. Here, electrons tunnel from border traps to the conduction band, interface traps and the valence band. Hence, the electrons that compensate positively charged defects leave the oxide [1,2].

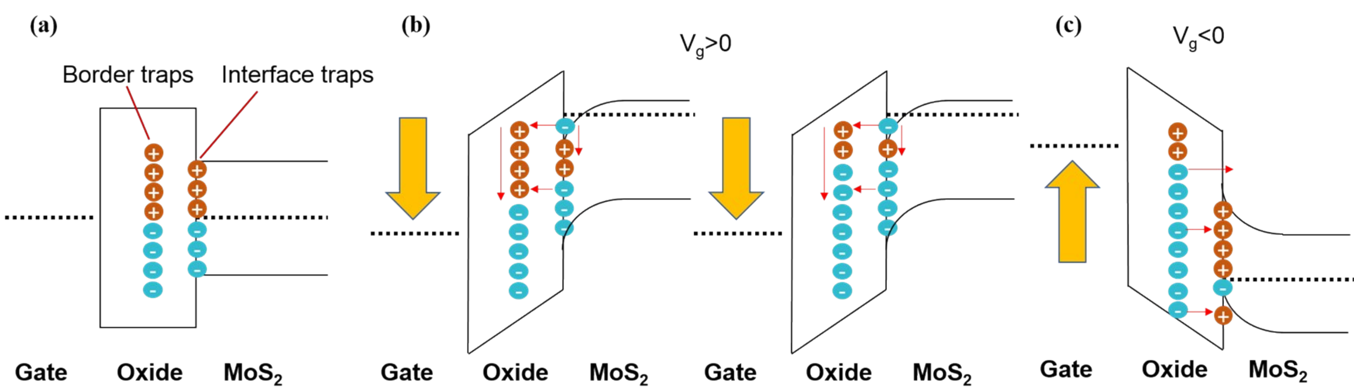

Fig. S6: Schematic plot of the border traps and interface traps mechanism model. [1]

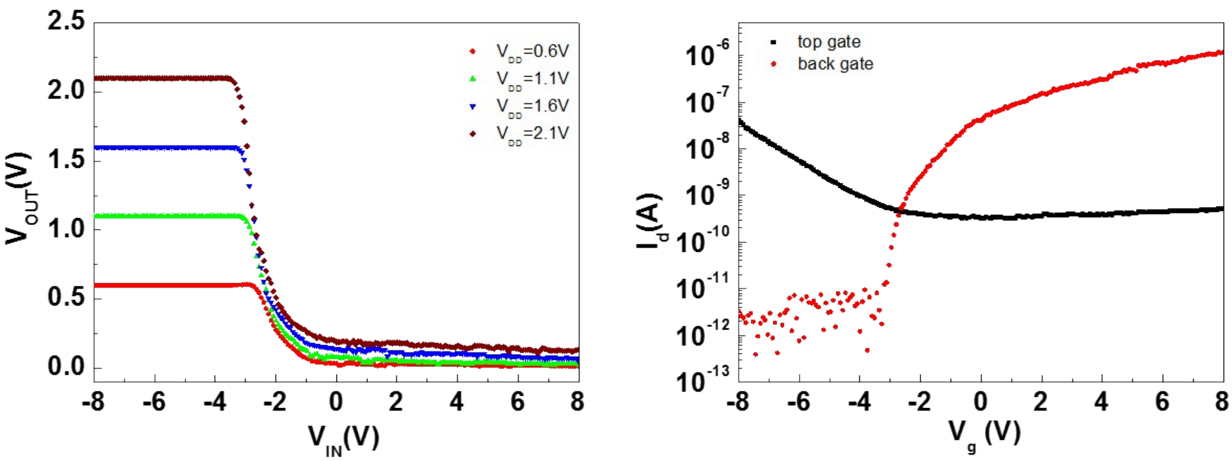

Fig. S7: The (Left) voltage transfer characteristics of another CMOS inverter as a function of V_d and the (Right) corresponding I_d-V_g characteristic of the top gate and back gate structure at $V_d = 1.1$ V.

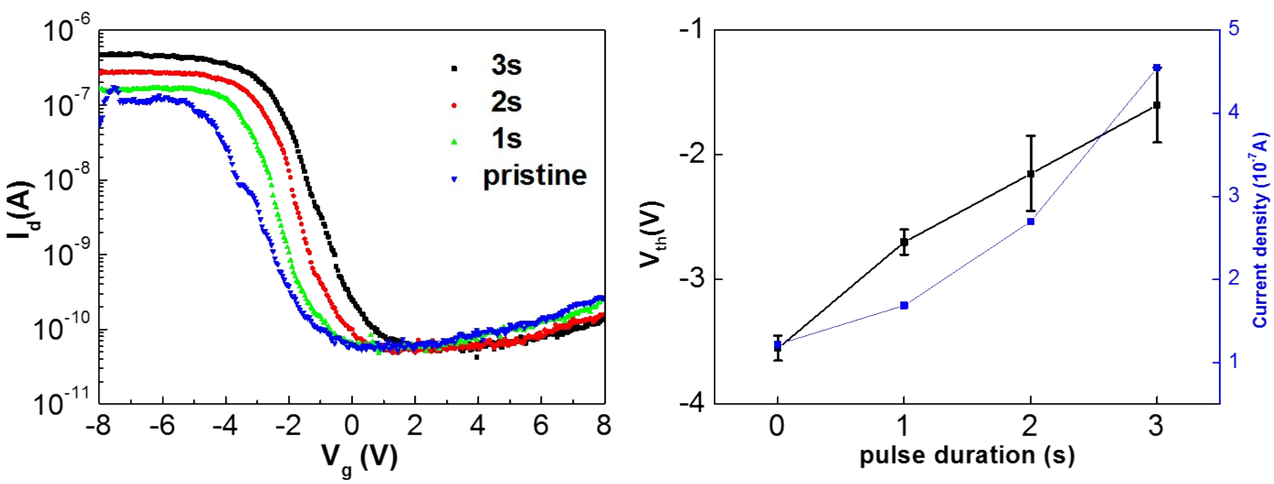

Fig. S8: The I_d-V_g characteristics of the other top gate structure as a function of gate voltage pulse duration (T_{GS}), and the corresponding current density and V_{th} tendency at different values of T_{GS}.

Table S1. The corresponding current density at -6V and V_{th} values in a fixed gate voltage pulse of -8V at various duration times while gate voltage sweep from -8V to 8V.

Pulse duration	Pristine	1s	2s	3s
Current density (A)at -6V	$1.22*10^{-7}$	$1.69*10^{-7}$	$2.7*10^{-7}$	$4.55*10^{-7}$
Threshold voltage (V_{th})	-3.55V	-2.7V	-2.15V	-1.6V

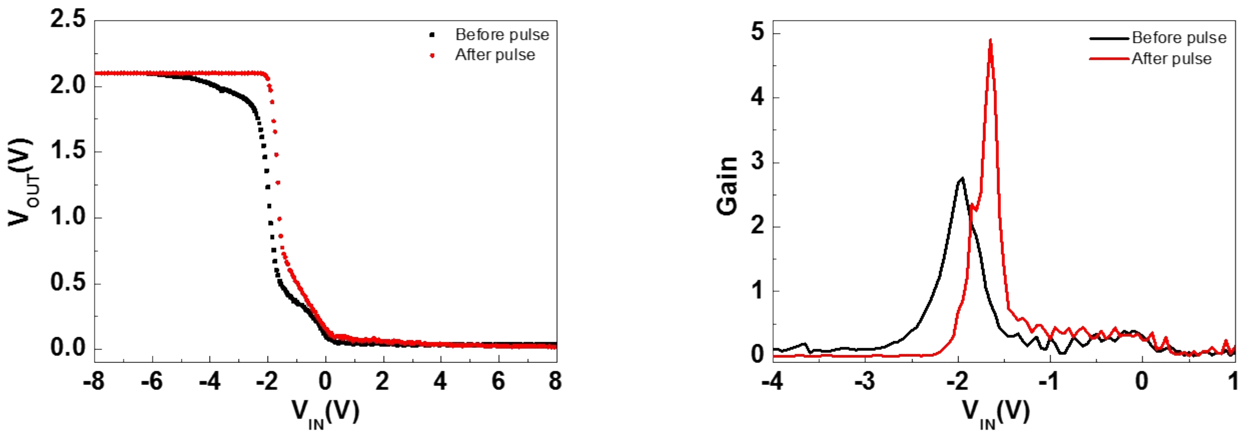

Fig. S9: (Left) The voltage transfer characteristics of the other CMOS inverter at V_d equal to 2.1 V. The black curve and red curve are the results before and after applying the gate voltage pulse (T_{GS}). (Right) The corresponding gain characteristics of the CMOS inverter at V_d equal to 2.1 V.

The details of the corresponding theoretical calculations

The semiconductor potential, ϕ_B, is described by the relation below:

$$\varphi_B = V_t ln\left(\frac{N_d}{n_i}\right) = 0.0259\ln\left(\frac{10^{11}}{10^{10}}\right) = 0.059V$$

and the maximum inversion width (X_{dT}) calculated below:

$$X_{dT} = \frac{\pi\varepsilon_s(2\psi_B)}{ln(4)eN_dT} = \frac{\pi * 11 * 8.85 * 10^{-14} * 2 * 0.059}{\ln(4) * 1.6 * 10^{-19} * \frac{10^{11}}{T} * T} = 1.62 * 10^{-5}cm$$

where T is the semiconductor thickness.

The charge in the depletion region at strong inversion, $|Q'_{SD(max)}|$, can then be determined using the formula:

$$\left|Q'_{SD(max)}\right| = eN_dX_{dT} = 1.6 * 10^{-19} * \frac{10^{11}}{4 * 10^{-9} * 10^2} * 1.62 * 10^{-5} = 6.48 * 10^{-7}C/cm^2$$

When applying a positive gate bias during the back gate operation, the ϕ_{ms} can be described by:

$$\varphi_{ms} = \varphi'_m - \left(\chi' + \frac{E_g}{2e} + \varphi_B\right) = 4.25 - \left(3.7 + \frac{1.4}{2} + 0.059\right) = -0.209V$$

The corresponding trapped oxide charges Q'_{SS} is calculated by the measured V_{th} of 6.4 V (Fig. 2(e)) through the V_{th} formula:

$$V_{th} = \left(\left|Q'_{SD(max)}\right| - Q'_{ss}\right)\left(\frac{t_{ox}}{\varepsilon_{ox}}\right) + \varphi_{ms} + 2\varphi_B$$

$$6.4 = \left(6.48 * 10^{-7} - Q'_{ss}\right)\left(\frac{30 * 10^{-9} * 10^2}{3.9 * 8.85 * 10^{-14}}\right) + (-0.209) + 2 * 0.059$$

$$Q'_{ss} = \left(6.48 * 10^{-7} + \frac{-6.4 + (-0.209) + 2 * 0.059}{\frac{30 * 10^{-9} * 10^2}{3.9 * 8.85 * 10^{-14}}}\right) = -9.87 * 10^{-8}C/cm^2$$

When applying a negative gate bias during the back gate operation, the ϕ_{ms} can be described by:

$$\varphi_{ms} = \varphi'_m - \left(\chi' + \frac{E_g}{2e} - \varphi_B\right) = 4.25 - \left(3.7 + \frac{1.4}{2} - 0.059\right) = -0.091V$$

In order to meticulously fit our experimental results, we assume the V_{th} is -8 V in the ambipolar characteristic of the device. The V_{th} can be described by:

$$V_{th} = \left(-\left|Q'_{SD(max)}\right| - Q'_{ss}\right)\left(\frac{t_{ox}}{\varepsilon_{ox}}\right) + \varphi_{ms} - 2\varphi_B$$

$$-8 = \left(-6.48 * 10^{-7} - Q'_{ss}\right)\left(\frac{30 * 10^{-9} * 10^2}{3.9 * 8.85 * 10^{-14}}\right) + (-0.091) - 2 * 0.059$$

$$Q'_{ss} = \left(-6.48 * 10^{-7} + \frac{8 - 0.091 - 2 * 0.059}{\frac{30 * 10^{-9} * 10^2}{3.9 * 8.85 * 10^{-14}}}\right) = 2.48 * 10^{-7} C/cm^2$$

Basically, Q'_{SS} is composed of bias-dependent border traps-induced charges (Q_V) which border traps related descriptions are shown in SF3 and bias-independent oxide charges (Q_S) which include fixed oxide charges, mobile ionic charges, and oxide trapped charges to name a few. Due to the bias-dependence of Q_V, the relationship of Q'_{SS} with Q_S and Q_V can be expressed using two different equations depending on the polarity of the applied gate bias. Using these equations,

$$Q'_{ss} = \begin{cases} Q_S - Q_V = -9.87 \times 10^{-8}\, cm^{-2} \\ Q_S + Q_V = 2.48 \times 10^{-7}\, cm^{-2} \end{cases},$$

By solving simultaneous equations above, Q_V is found to be about 7.49×10^{-8} C/cm^2, while Q_S is about 3.46×10^{-7} C/cm^2.

For the top gate operation, we also considered the influence of border traps in calculating the top gate dielectric layers' charges accordingly. When a positive bias is applied, the ϕ_{ms} can be described by:

$$\varphi_{ms} = \varphi'_m - \left(\chi' + \frac{E_g}{2e} + \varphi_B\right) = 4.5 - \left(3.7 + \frac{1.4}{2} + 0.059\right) = 0.041V$$

Note that electron affinity, χ', in the SiO_2-MoS_2 interface for the top gate structure is used for the calculation.

For the same reason as in the back gate operation, V_{th} was assumed to be 8 V.

$$V_{th} = \left[\left|Q'_{SD(max)}\right|\left(\frac{t_{ox1}}{\varepsilon_{ox1}} + \frac{t_{ox2}}{\varepsilon_{ox2}}\right) - Q'_{ss1}\left(\frac{t_{ox1}}{\varepsilon_{ox1}}\right) - Q'_{ss2}\left(\frac{t_{ox2}}{\varepsilon_{ox2}}\right)\right] + \varphi_{ms} + 2\varphi_B$$

$$8 = \left[6.48 * 10^{-7}\left(\frac{10 * 10^{-9} * 10^2}{23 * 8.85 * 10^{-14}} + \frac{5 * 10^{-9} * 10^2}{3.9 * 8.85 * 10^{-14}}\right) - Q'_{ss1}\left(\frac{t_{ox1}}{\varepsilon_{ox1}}\right) - Q'_{ss2}\left(\frac{t_{ox2}}{\varepsilon_{ox2}}\right)\right] + 0.041 + 2 * 0.059$$

$$8 = 1.25 - Q'_{ss1}\left(\frac{t_{ox1}}{\varepsilon_{ox1}}\right) - Q'_{ss2}\left(\frac{t_{ox2}}{\varepsilon_{ox2}}\right) + 0.041 + 2 * 0.059$$

$$8 = 1.25 - (Q_{S1} - Q_{V1})\left(\frac{t_{ox1}}{\varepsilon_{ox1}}\right) - (Q_{S2} - Q_{V2})\left(\frac{t_{ox2}}{\varepsilon_{ox2}}\right) + 0.041 + 2 * 0.059$$

We assumed the quantities $V_V = Q_{V1}(t_{ox1}/\varepsilon_{ox1}) + Q_{V2}(t_{ox2}/\varepsilon_{ox2})$ and $V_S = Q_{S1}(t_{ox1}/\varepsilon_{ox1}) + Q_{S2}(t_{ox2}/\varepsilon_{ox2})$. Here, V_V and V_S are both contributed by the top gate structure's HfO_2 (Q_{V1} and Q_{S1}) and SiO_2 (Q_{V2} and Q_{S2}) dielectric layers.

$\Rightarrow -V_S + V_V = 6.591V$

Meanwhile, in the negative bias condition, the ϕ_{ms} can be described by:

$$\varphi_{ms} = \varphi'_m - \left(\chi' + \frac{E_g}{2e} - \varphi_B\right) = 4.5 - \left(3.7 + \frac{1.4}{2} - 0.059\right) = 0.159V$$

$$V_{th} = \left[-\left|Q'_{SD(max)}\right|\left(\frac{t_{ox1}}{\varepsilon_{ox1}} + \frac{t_{ox2}}{\varepsilon_{ox2}}\right) - Q'_{ss1}\left(\frac{t_{ox1}}{\varepsilon_{ox1}}\right) - Q'_{ss2}\left(\frac{t_{ox2}}{\varepsilon_{ox2}}\right)\right] + \varphi_{ms} - 2\varphi_B$$

while the measured V_{th} is -4.8 V (Fig. 2(e)) is applied to the V_{th} formula:

$$-4.8 = \left[-6.48 * 10^{-7}\left(\frac{10 * 10^{-9} * 10^2}{23 * 8.85 * 10^{-14}} + \frac{5 * 10^{-9} * 10^2}{3.9 * 8.85 * 10^{-14}}\right) - Q'_{ss1}\left(\frac{t_{ox1}}{\varepsilon_{ox1}}\right) - Q'_{ss2}\left(\frac{t_{ox2}}{\varepsilon_{ox2}}\right)\right] + 0.159 - 2 * 0.059$$

$$-4.8 = -1.25 - Q'_{ss1}\left(\frac{t_{ox1}}{\varepsilon_{ox1}}\right) - Q'_{ss2}\left(\frac{t_{ox2}}{\varepsilon_{ox2}}\right) + 0.147$$

$$-4.8 = -1.25 - (Q_{S1} + Q_{V1})\left(\frac{t_{ox1}}{\varepsilon_{ox1}}\right) - (Q_{S2} + Q_{V2})\left(\frac{t_{ox2}}{\varepsilon_{ox2}}\right) + 0.147$$

We also assumed the quantities $V_V = Q_{V1}(t_{ox1}/\varepsilon_{ox1}) + Q_{V2}(t_{ox2}/\varepsilon_{ox2})$ and $V_S = Q_{S1}(t_{ox1}/\varepsilon_{ox1}) + Q_{S2}(t_{ox2}/\varepsilon_{ox2})$.

$\Rightarrow -V_S - V_V = -3.697V$

$$V_{total} = \begin{cases} -V_s + V_V = 6.591\ V \\ -V_s - V_V = -3.697\ V \end{cases}$$

By solving simultaneous equations above, we get V_V at 5.144V, and V_S equal to -1.447V.

References

[1] D. K. Schroder, *Electrical Characterization of Defects in Gate Dielectrics.* In Defects in Microelectronic Materials and Devices; D. M. Fleetwood, S. T. Pantelides, R. D. Schrimpf, Eds.; CRC Press, 2009.

[2] D.M. Fleetwood, Border traps and bias-temperature instabilities in MOS devices. *Microelectronics Reliability* ,2018,**80**,266-277.