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Supplementary Information for

Aluminium and Zinc co-doped $CuInS_2$ QDs for enhanced trion modulation in monolayer WS_2 toward improved electrical properties

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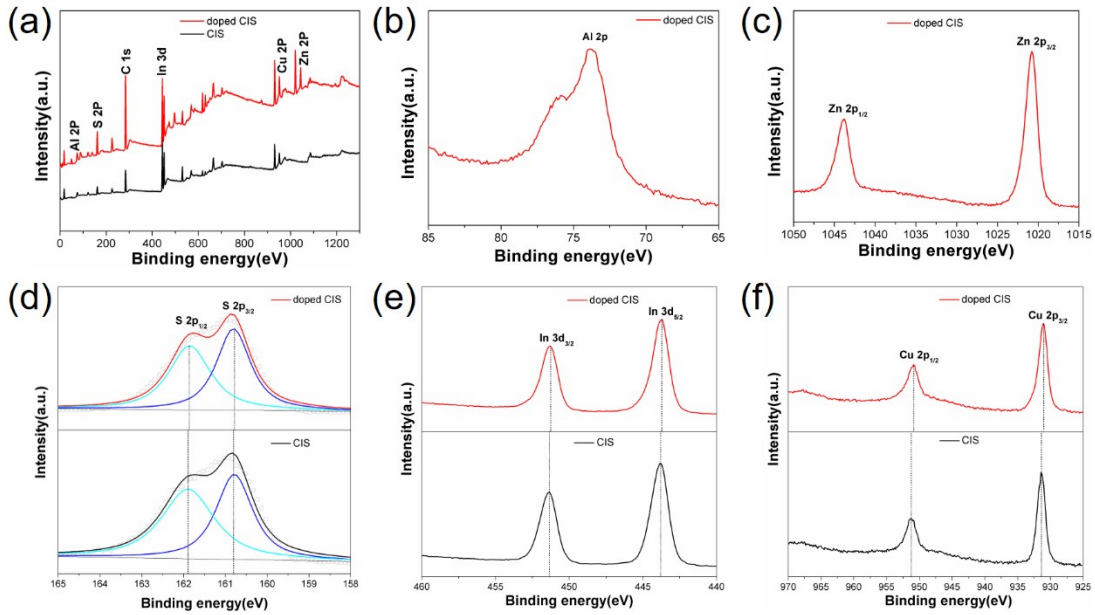


Fig. S1 (a) Full spectra of CIS and doped CIS QDs; (b) Al 2p and (c) Zn 2p spectra of doped CIS QDs; The comparison of Cu 2p (d), S 2p (e) and In 3d (f) spectra in CIS and doped-CIS QDs.

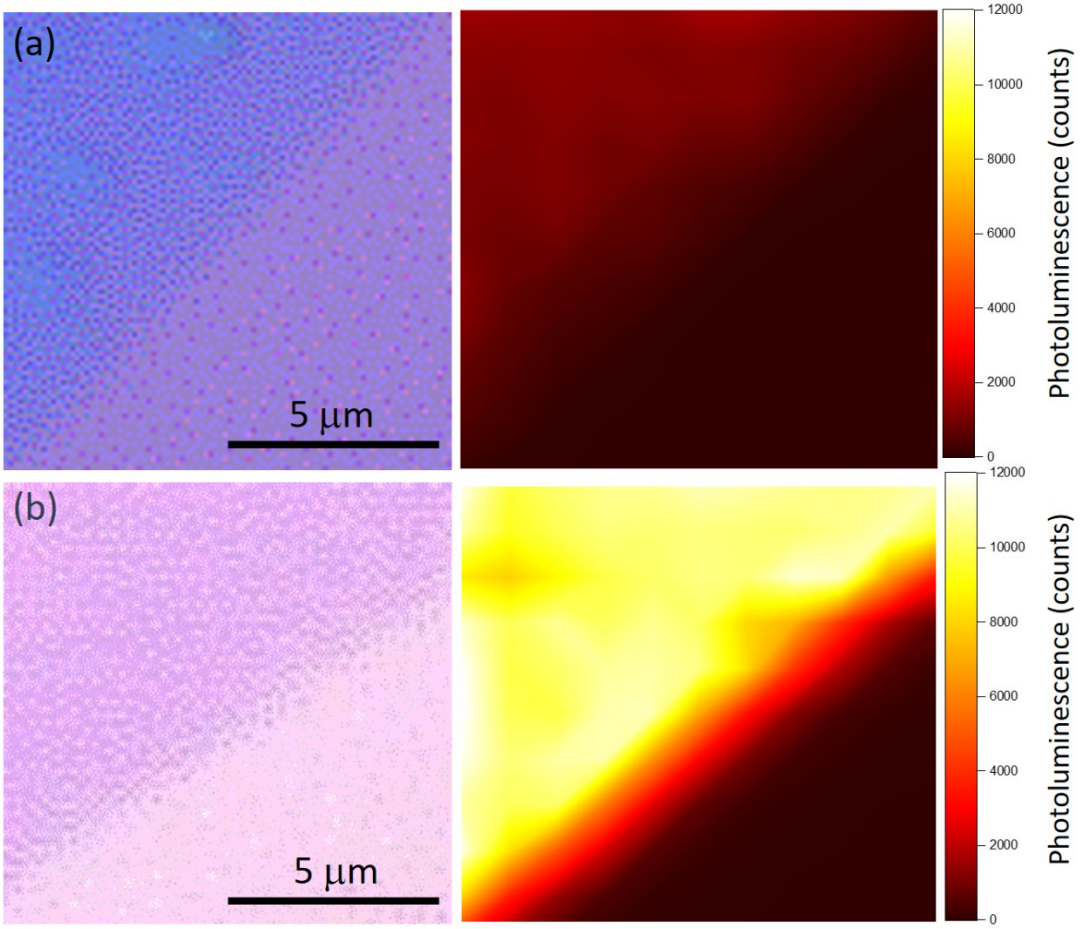
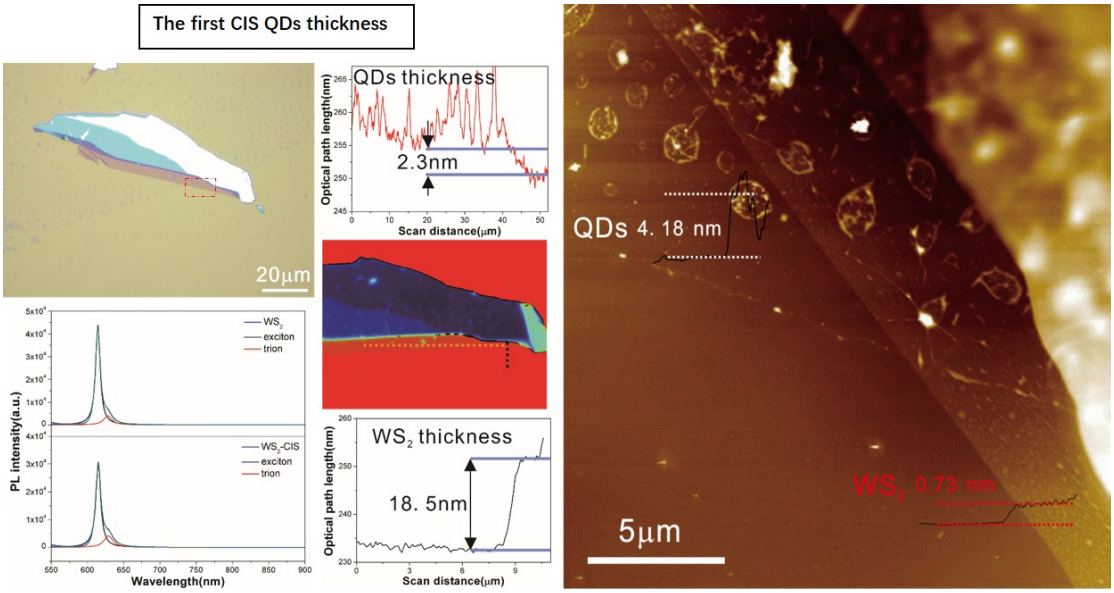
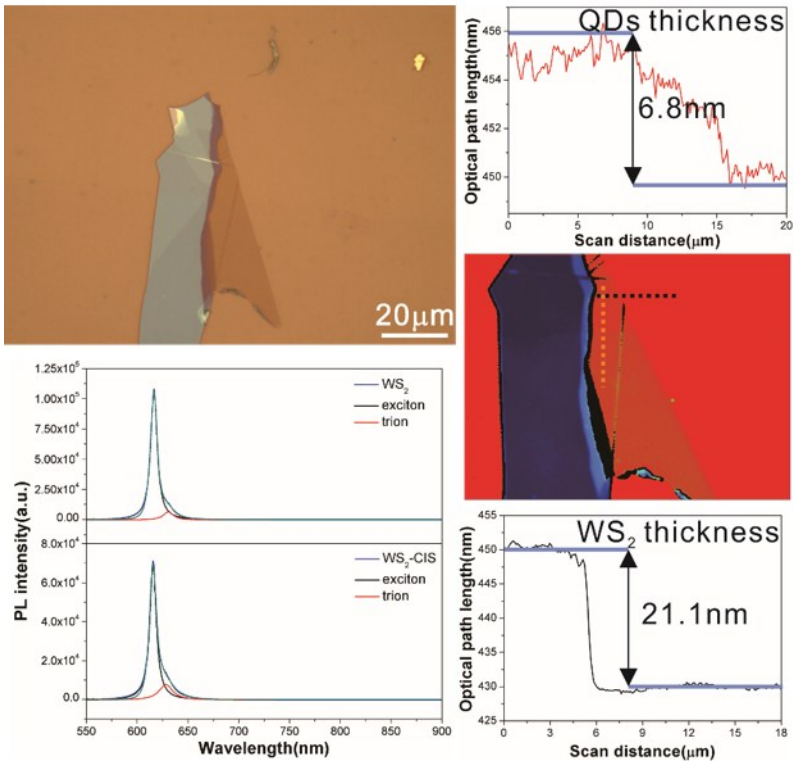


Fig. S2. The optical image and corresponding PL intensity mapping results of (a) CIS QDs and (b) doped CIS QDs.

The first CIS QDs thickness



The second CIS QDs thickness



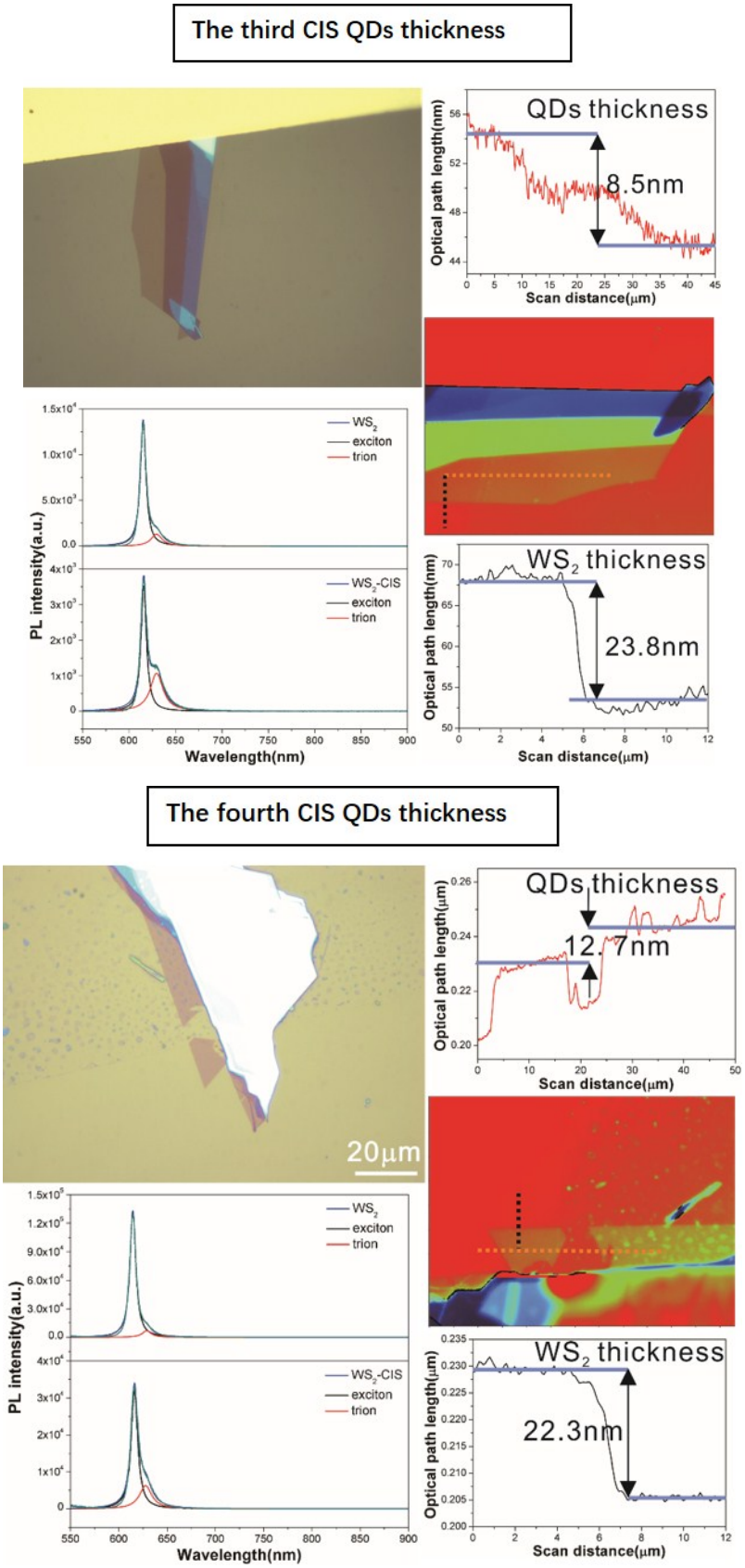
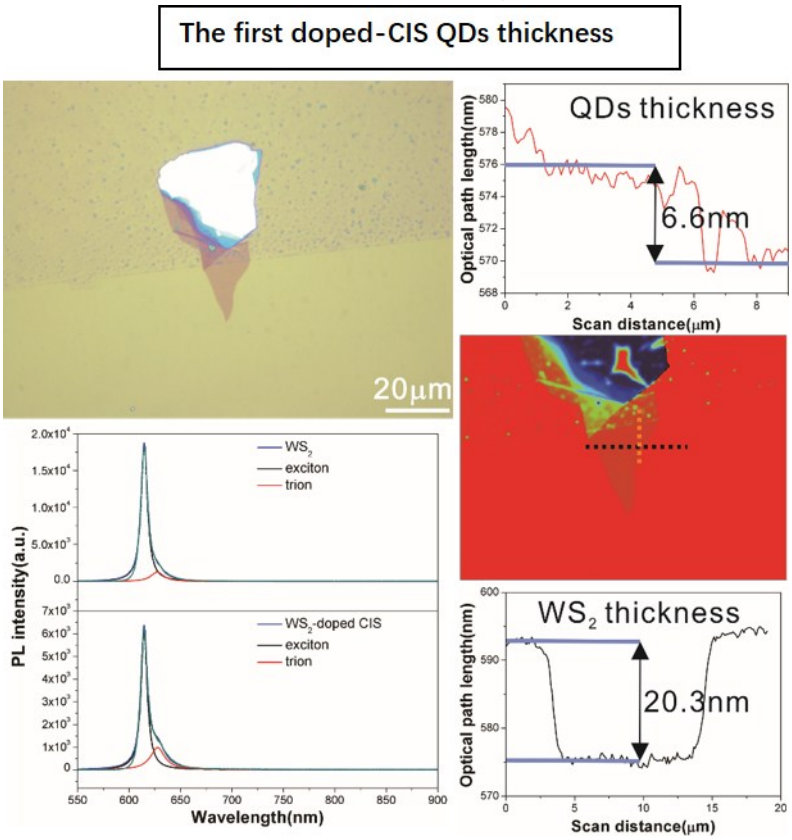
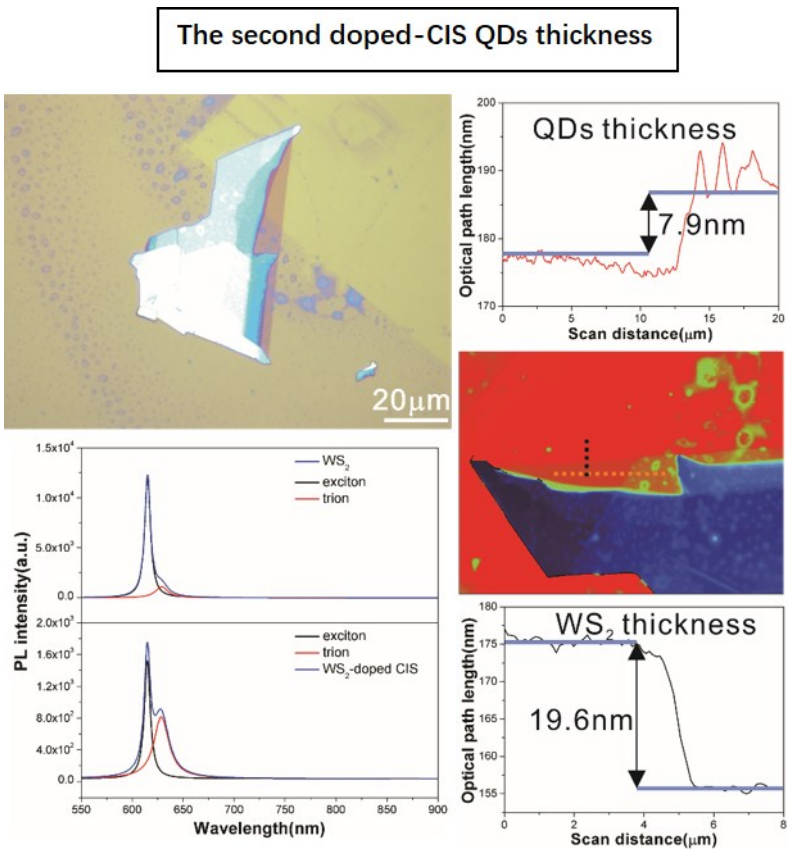


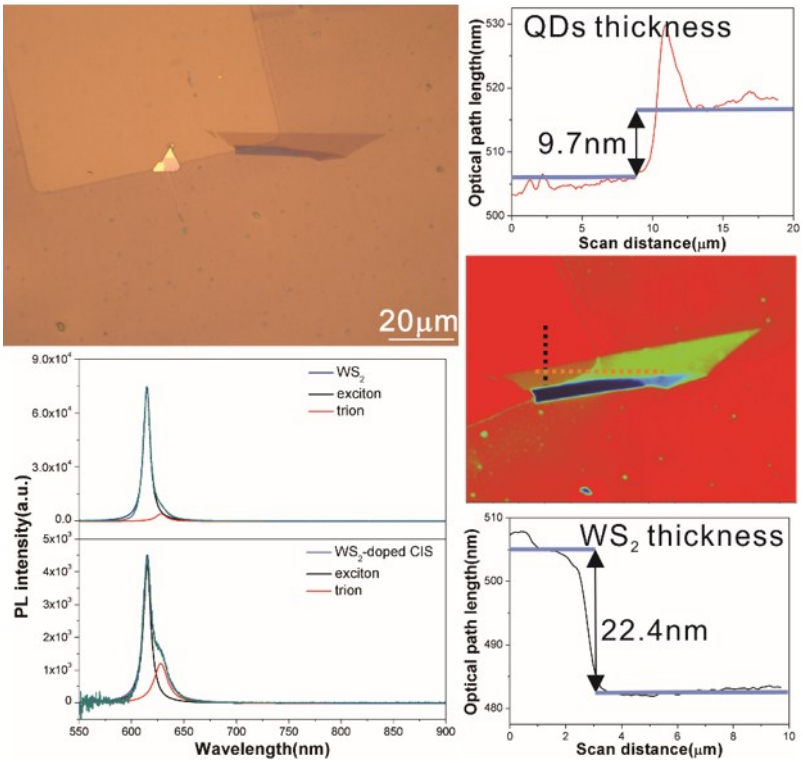
Fig. S3. The fabricated WS_2-CIS chips with different CIS QDs thickness, including optical image, PSI measurement, and the corresponding PL spectra without and with CIS QDs modification. The CIS QDs thickness is in the range of 2.3 to 12.7 nm. It should be noted that OPL value of 2.3 in first

CIS QDs thin film correspond to 4.18 nm actual CIS thickness, and OPL value of 18.5 nm in bare WS_2 correspond to the actual 0.73 nm thickness of monolayer WS_2.

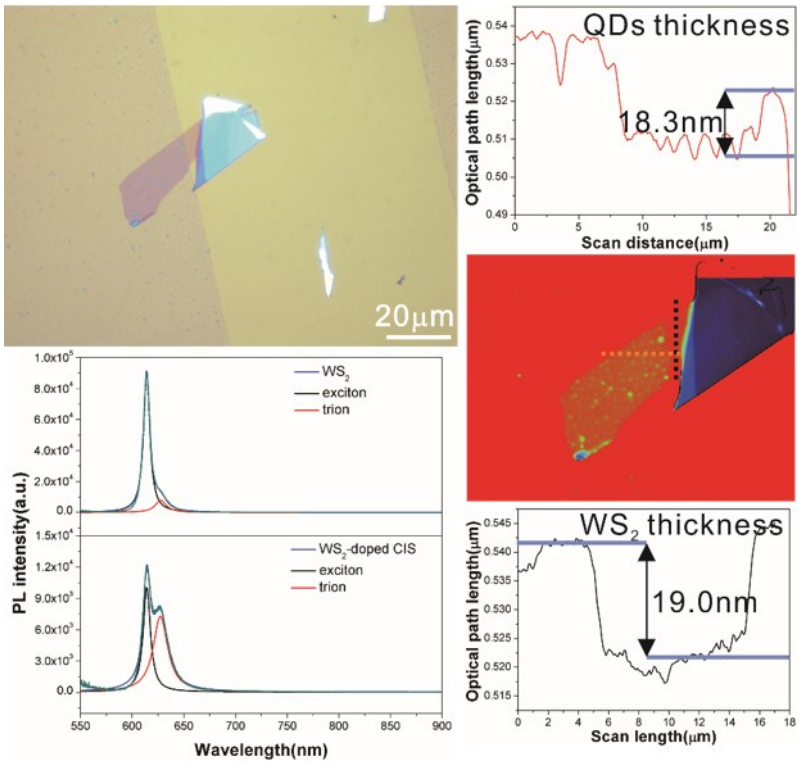




The third doped-CIS QDs thickness



The fourth doped-CIS QDs thickness



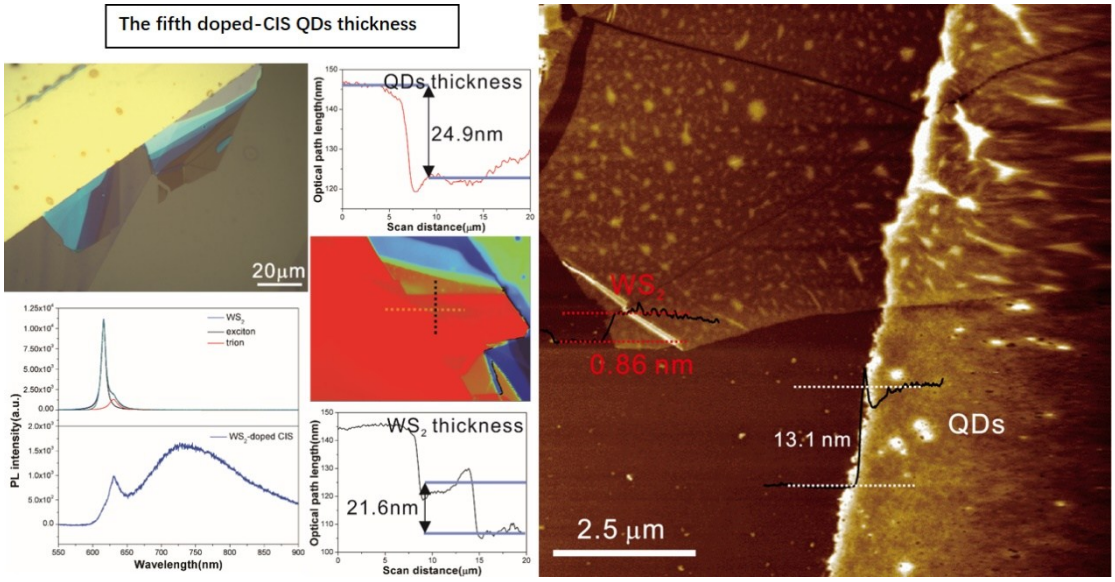


Fig. S4. The fabricated WS_2-doped CIS chips with different doped CIS QDs thickness, including optical image, PSI measurement, and the corresponding PL spectra without and with doped-CIS QDs modification. The doped-CIS QDs thickness is in the range of 6.6 to 24.9 nm. It should be noted that OPL value of 24.9 in fifth doped-CIS QDs correspond to 13.1 nm actual doped-CIS thickness, and OPL value of 21.6 nm in bare WS_2 correspond to the actual 0.86 nm thickness of monolayer WS_2.

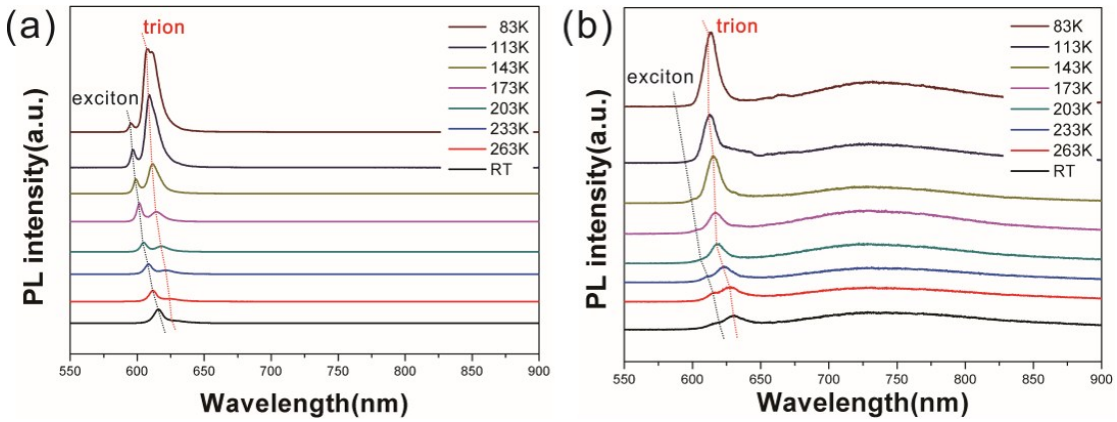


Fig. S5. Temperature-dependent PL spectra of (a) bare WS_2 and (b) WS_2-doped CIS with 24.9 nm QDs thickness. (the fifth doped-CIS thickness)

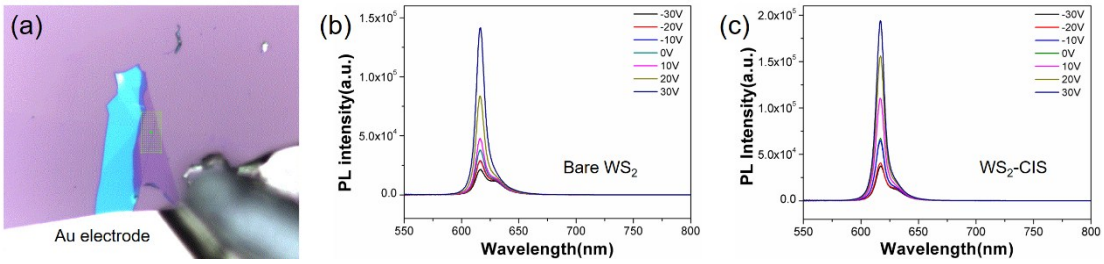


Fig. S6. (a) Optical image of WS_2-CIS for gate-dependent testing. (b) PL spectra of bare WS_2 under different gate voltage. (c) PL spectra of WS_2-CIS under different gate voltage.

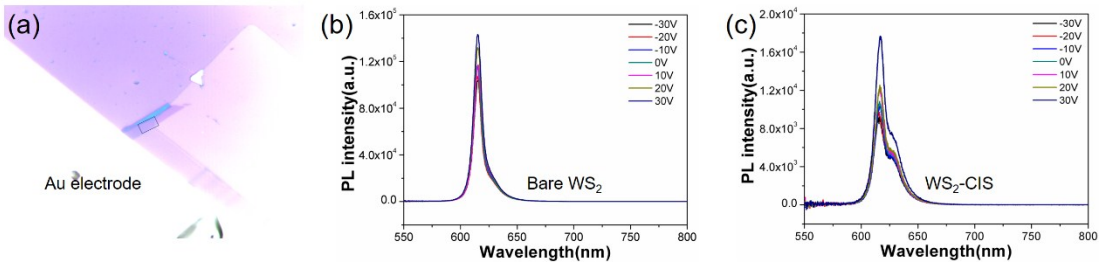


Fig. S7. (a) Optical image of WS_2-doped CIS for gate-dependent testing. (b) PL spectra of bare WS_2 under different gate voltage. (c) PL spectra of WS_2-doped CIS under different gate voltage.

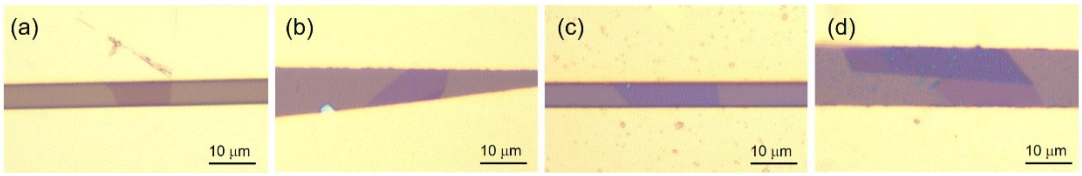


Fig. S8. Optical images of as-fabricated FET chips. (a) bare WS_2; (b) WS_2-CIS; (c) WS_2-doped CIS 1; (d) WS_2-doped CIS 2.