Supplementary Information for

Highly scalable resistive switching memory cells using pore-size-controlled nanoporous alumina templates

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**Fig. S1** Process steps for the synthesis of nanoporous AAO templates. FE-SEM images after (a) the electro-polishing step, (b) the first anodization, (c) the removal of the AAO layer, and (d) the second anodization.
Fig. S2 Tilted FE-SEM images of (a) the AAO template filled with polystyrene (PS), (b) the AAO nanotemplate placed on the conductive substrate after the removal of PS, (c) deposition of HfO$_2$ on the conductive substrate with the AAO nanotemplate, and (d) the HfO$_2$ nanodot array after the removal of the AAO nanotemplate.
Fig. S3 AFM images of the partially scratched samples for the (a) plan view and (b) three-dimensional view of the Au/HfO₂ nanodots, and (c) the AFM depth (thickness) profile along with line AB in Figure S3 (a).
**Fig. S4** Typical forming process of the nanoscale resistive memory devices.