Supporting Information

**Damage-free Hybrid Encapsulation of Organic Field-Effect Transistors to Reduce Environmental Instability**

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**Fig. S1.** AFM topographies of 50 nm thick pentacene films on the PS/SiO$_2$ dielectrics after annealing at various temperatures for 1 h: (a) 30 °C; (b) 60 °C; (c) 90 °C; (d) 120 °C; (e) 150 °C; (f) 180 °C.
Fig. S2. 2D X-ray $\theta$/$2\theta$ scanning patterns showing the overall crystal structures of 50 nm thick pentacene films on the PS/SiO$_2$ dielectrics after annealing at various temperatures for 1 h. (Based on two different X-ray modes: GIXD and $\theta$/$2\theta$ scanning, it was found that the 120 $^\circ$C sample contained two different types of “bulk phase”, located at different film levels.)
Fig. S3. $I_D-V_G$ transfer characteristics of a top-contact electrode pentacene OFET (with channel length $L = 100 \, \mu m$ and width $W = 1500 \, \mu m$) employing a PI/SiO$_2$ dielectric ($V_{DS} = -40 \, V$).

Fig. S4. AFM surface topographies of a PS/SiO$_2$ dielectric before (a) and after (b) SiO$_x$ layer coating.
Fig. S5. AFM topographies of SiO$_x$-capped pentacene films on PI/SiO$_2$ dielectrics after thermal annealing at various temperatures for 1 h.
Fig. S6. $I_D-V_G$ transfer curves of SiO$_x$-capped pentacene OFETs employing PS/SiO$_2$ dielectrics before and after aging in various environments: acetone, DMF, and O$_2$ plasma ($V_D = -40$ V).

Fig. S7. $I_D-V_G$ transfer curves of SiO$_x$-capped pentacene OFETs employing PS/SiO$_2$ dielectrics before and after the deposition of a 50 nm thick AlO$_x$-layer by using (a) RF magnetron sputtering and (b) PEALD ($V_D = -40$ V).
Fig. S8. (a) Chemical structure of the CYTOP™ polymer. (b) Cross-sectional transmission electron microscopy (TEM) image of pentacene OFET device encapsulated by SiOₓ-AlOₓ bilayer.