

B816575K_supplementary_revd.doc
December 3, 2008

*Supplementary Information
for*

**Rapid and inexpensive fabrication of polymeric microfluidic devices via
toner transfer masking**

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Supplementary Information

Brass etching. The brass substrates were etched in a 20% solution (% w/v) of ammonium persulfate (APS, $(\text{NH}_4)_2\text{S}_2\text{O}_8$), which is commercially available at electronics suppliers. During etching, the brass sheets were weighed on a fine balance in increments over a 90 min period. The average dissolution rate was found to be $0.428 \pm 0.047 \text{ mg cm}^{-2} \text{ min}^{-1}$. As discussed in the text, this data also revealed that the mass removed during etching was directly proportional to the etch depth, with a linear correlation coefficient of 0.99993 and a y-intercept of $-0.09534 \pm 0.10819 \text{ }\mu\text{m}$, essentially zero (Supplementary Fig. S1a). This allowed the brass weight to be used as a simple and accurate indicator of microfluidic channel depth via Equation 1 (see text). Using a profilometer, the brass surface roughness was also measured as a function of etch depth (Fig. S1b). As shown in the figure, the roughness increased linearly with the etch depth, from $\sim 0.2 \text{ }\mu\text{m}$ roughness at $\sim 2 \text{ }\mu\text{m}$ depth to $\sim 1.5 \text{ }\mu\text{m}$ roughness at $\sim 40 \text{ }\mu\text{m}$ depth. The surface roughness was shown to decrease following the final brass-polishing step using commercially available metal polish (Brasso®), although post-polish surface roughness data was not collected extensively.

It should be noted that APS was not the most obvious choice for a brass etchant solution. In fact, ferric chloride (FeCl_3) etchants (also commercially available) are capable of etching brass much more rapidly, and these are the most commonly used etchants for home-made electrical circuits. Unfortunately, etching brass with FeCl_3 etchants resulted in oxide film formation³⁸, which was visually obvious as a dull, dark brown surface coating almost immediately following the onset of etching. These films caused anisotropic etching near the toner patterns, and the effect was apparently accelerated by stirring or shaking the solution. This problem is avoided using APS, since ammonia forms soluble complexes with Cu^{1+} or Cu^{2+} as the persulfate ions oxidize the copper³⁸. Presumably, this prevents disproportionation of Cu^{1+} into Cu^0 and Cu^{2+} . On the other hand, surface roughness was

increased by etching brass in APS (see Fig. S1b). It was found that this surface roughness could be greatly reduced by simply immersing the brass in a ferric chloride etchant for 5 minutes, without stirring, followed by a brass-polishing step using commercially available metal polish (Brasso®).

Resolution tests. As noted in the text, a resolution test pattern (Supplementary Fig. S2) was designed and printed in triplicate, and a wide-field microscope was used to collect digital images of the printed patterns on the paper substrate. The pattern was designed in Adobe Illustrator then transferred to Adobe Photoshop and rasterized for compatibility with the laser printer (to avoid aliasing of the images). As shown in Fig. S2, the test pattern consisted of 1- to 24-pixel (21.2 to 508.0 μm) line widths and 1- to 12-pixel (21.2 to 254.0 μm) line spacing, in both vertical and horizontal configurations.

Via fabrication for three-dimensional networks. For via construction, the lower and upper layer toner patterns consisted of a typical channel network design, while the via layer pattern consisted of regions designed to intersect with the pre-etched lower pattern (Supplementary Fig. 3). Briefly, the lower layer master was fabricated at the desired channel thickness using TTM, and the toner was removed. Next, the via layer pattern was printed onto paper, and this pattern was transferred to the lower layer pattern using heat and pressure. Toner was transferred only to the regions in which the via layer pattern intersected with the raised, un-etched, features. This method allowed the deposition of very small regions of toner onto pre-existing, raised features. Upon further etching to the desired depth, the small toner regions protected the raised brass, while the remainder of the raised brass was etched further. Finally, the upper layer pattern was fabricated at the desired channel thickness using TM, and the toner was removed. Two masters resulted from this method. The via-forming master (for

the lower microfluidic channels) consisted of multiple depths, with small raised regions to serve as via masters. The upper fluidic master consisted simply of a channel network of a single depth, to serve as the master for the upper microfluidic channels.

As noted in the text, the three-dimensional channel patterns could then be fabricated without the use of a spin-coater or cleanroom facility. Similar to the method used to fabricate valves, a transparency film covered by a sheet of glass was clamped onto the via-forming master. Using a modification of the method developed by Beebe and coworkers²⁶, PDMS was poured over the via-forming master, and the master/transparency/glass assembly was clamped tightly and heated to PDMS curing temperature (70 °C, 1-2 h). Next, a thick (5-mm) layer of PDMS was cured over the upper fluidic master. The fluidic and via-forming layers could be joined by either partial curing and annealing¹⁸ or by plasma oxidation and adhering¹⁸, and these joined layers were sealed to a glass slide by plasma oxidation and adhering. Small vias were created with this technique, with an average volume of 2.5 ± 0.6 nL (see **Fig. 3d** in text).

Cost analysis. Consumable costs of the TTM method were compared to that of master fabrication by standard photolithography. Costs of the consumable materials purchased for TTM in this work (brass strips, persulfate and ferric chloride copper etchants, a printer cartridge, and metal polish) were tabulated, then adjusted for amounts needed to fabricate a 6.45 cm^2 (1.00 in^2) brass master. The total cost of consumables to fabricate one master of this size was estimated to be \$0.85— or, more roughly $< \$1$, as noted in the manuscript. By comparison, consumables for standard photolithography would include (at minimum) SU-8 photoresist, SU-8 developer, and a silicon wafer. These costs were tabulated and adjusted as well, amounting to \$10.68 per master, over an order of

magnitude higher cost than that of the TTM method. In fact, the cost ratio (photolithography cost per master to TTM cost per master) was calculated here to be 12.6.

It is important to note that this cost analysis ignores equipment costs, which should, again, be much larger with standard photolithography. In the standard methods, these types of costs would include a photomask for each chip design, a specialized UV flood-exposure unit, spin-coaters, a hot-plate (or oven), and costly maintenance of cleanroom facilities. In comparison to the minimal equipment needed for the TTM method, these items would undoubtedly add to the cost ratio calculated above.

Supplementary Figures and Legends

Figure S1. (a) Brass etch depth during etching with 20% APS, measured using a profilometer, plotted as a function of removed mass from the brass sheet during etching. The linear relationship (dotted line), with a y-intercept of essentially zero, reveals that the removed mass (Δm in Equation 1 in text) can be used as a simple indicator of etch depth and, thus, microfluidic channel depth after molding. Error bars represent the standard deviation about the mean. (b) The brass surface roughness was shown to be linear with etch depth, before the polishing step.

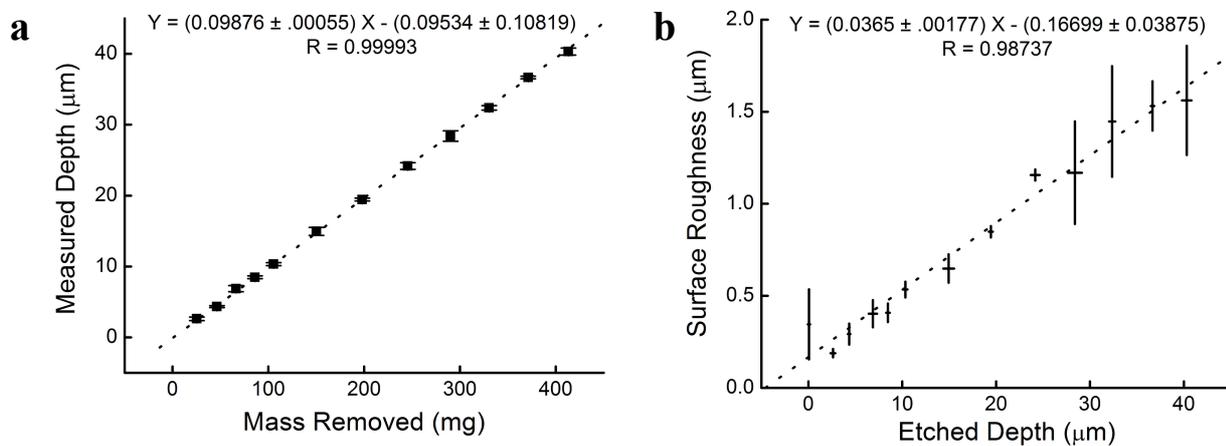


Figure S2. Resolution test pattern used for measurement of line widths and line spacing of toner printed on photo paper as well as toner transferred to brass substrates. The pattern, which was designed in Adobe Illustrator then transferred to Adobe Photoshop and rasterized, included vertical and horizontal line widths between 1 and 24 pixels (21.2 to 508.0 μm) and spacing from 1 to 12 pixels (21.2 to 254.0 μm).

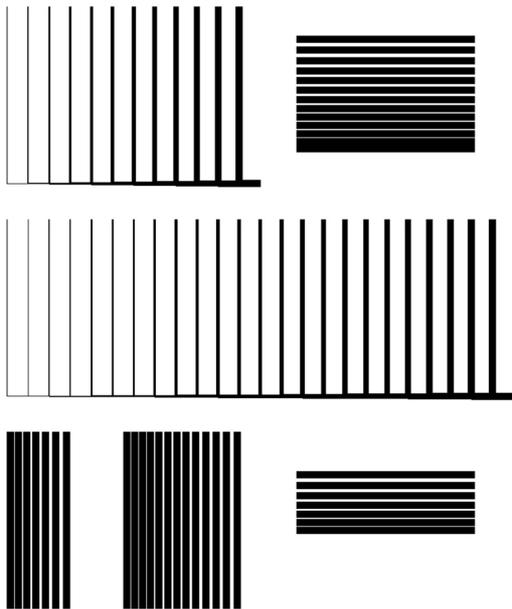


Figure S3. Via mask patterns used for TTM fabrication of three-dimensional channel networks. Vias were formed at the intersections of the lower layer pattern (left) and via pattern (middle), resulting in low-volume connectors between upper (pattern on right) and lower fluidic channel layers in the final devices (see **Fig. 3d** in text).

