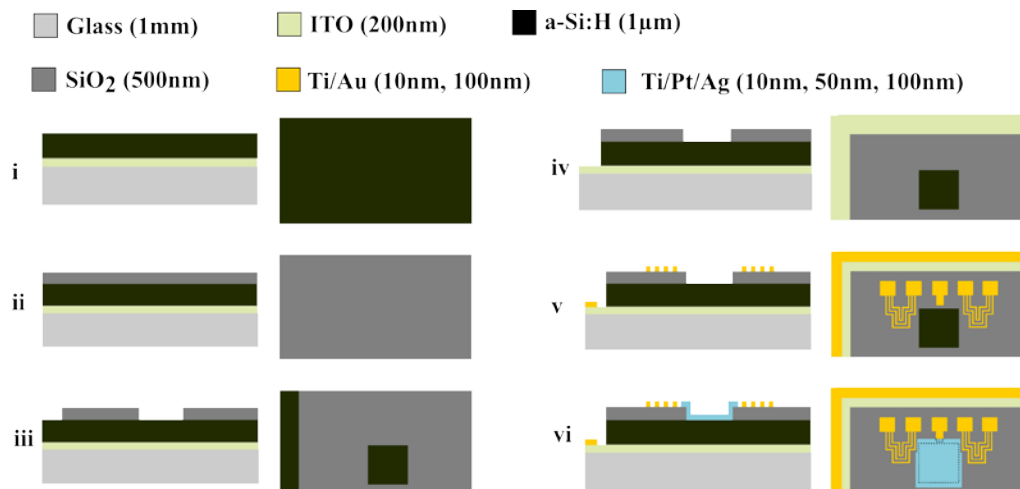


Microfabrication procedure



Amorphous silicon chip consisting of a 200nm layer of ITO on glass with a 1µm-thick top layer of hydrogenated amorphous silicon (a-Si:H) (i). 500nm of silicon dioxide (SiO₂) are deposited by plasma enhanced chemical vapor deposition (PECVD) (ii). SiO₂ is wet-etched in the chip periphery and in the reconfigurable areas using a 6:1 buffer oxide etch (BOE) solution (iii). RIE-etching of a-Si:H in the chip periphery (iv). Contact pads and microheaters are fabricated by e-beam evaporation (10nm titanium, 100nm gold) and subsequent lift-off (v). Reconfigurable areas are fabricated through e-beam evaporation (10nm titanium, 50nm platinum, and 100nm silver) and lift-off (vi).