Electronic Supplementary Material (ESI) for Lab on a Chip

SUPPORTING INFORMATION

Ion channel recordings on an injection molded polymer chip

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CONTENTS

1. LEAK SUBTRACTION

The total current response to a voltage step recorded from a cell in voltage clamp mode comprises two current components: a component with amplitude that has a non-linear dependence on the voltage step and a component with amplitude that has a linear dependence on the voltage step,

$$I_{tot}(t) = I_l(t) + I_i(t) \quad \text{[I]}$$

where $I_{tot}(t)$ is the total current signal evoked by the depolarizing voltage step V_t , $I_l(t)$ is the linear current amplitude response and $I_i(t)$ is the ionic non-linear current response which is assumed to have passed through the voltage-gated ion channels.[1, 2] The linear current response consists of capacitive currents, associated with the rapid change in voltage, plus a DC leakage current. The leakage current and the amplitude of the capacitive current response are both linearly related to the size of the voltage step. The linear component can be subtracted from the total current by means of a method called leak subtraction, leaving only the ionic current. It is possible to calculate the leak subtraction current $I_{sub}(t)$ produced by a small 10 mV step, in a voltage range where voltage-gated channels are closed (and hence where $I_i(t)$ is zero), and to scale it up with the ratio of the amplitudes of the two stimuli,

$$I_{sub}(t) = I_c(t)\frac{V_t}{V_c} \quad \text{[II]}$$

where $I_c(t)$ is the current evoked by the 10 mV test pulse amplitude V_c. The subtraction current $I_{sub}(t)$ can then be subtracted from the recorded signal, leaving the ionic current,

$$I_i(t) = I_{tot}(t) - I_{sub}(t) \quad \text{[III]}$$

Subtraction of capacitive currents may reveal small current contributions that would otherwise be hard to identify especially the one happening very rapidly after the start of the pulse. Figure S1 shows an example of a record of sodium current that has been leak subtracted.

2. PERFUSION OF BLOCKING COMPOUND

In order to study the lidocaine dose response on sodium channels, we needed to know the exact concentration that was delivered to the cell during each perfusion. A model made in COMSOL® showed that our system was able to deliver close to 100 % of the lidocaine present in solution. The diffusion coefficient for lidocaine (2.21×10^{-10} m^2/s) was calculated from the Stokes-Einstein equation with the assumptions that lidocaine molecules are comparable to small spherical molecules and that their radius can be derived from the molecular weight (234.4 g/mol). The viscosity of the extracellular electrolyte solution was assumed the same as water,

$$D = \frac{kT}{6\pi r\eta} \qquad \text{[IV]}$$

where k is the Boltzman costant, η is the viscosity of water, T is the absolute temperature and r is the hydraulic radius of the lidocaine molecules. In order to evaluate the delivery of lidocaine to the cell, the entire channel geometry was set up as a model in COMSOL®. The flow rates in the main channel and the perfusion channel, respectively, were estimated from both the speed at which the syringes containing lidocaine were operated during the experiments and the observed flow velocity in the main channel. The latter was in the order of 1 mm/s, and from this the flow in the main channel was estimated to be 4 nL/s. The flow in the perfusion channel was estimated to be roughly 20 % higher than this, i.e. 4.8 nL/s. These values were used as boundary conditions in the model at the channel inlets, along with the assumption of steady state flow.

3. FABRICATION OF THE POLYMER DEVICE

The shaped silicon masters used for forming the metal shims for both types of devices were fabricated using a combination of photolithography, deposition and etching steps, as shown in Figure S2. The only difference between type A and type B was the etching process employed to form the patching capillaries: Bosch reactive ion etching for type A devices and a continuous reactive ion etching for type B devices. We started from 100 mm, <100 >, single side polished, 525 µm thick silicon wafers. A chemical treatment with hexamethyldisilazane (HMDS) before any spin coatings was used to promote the adhesion of the resist; the treatment was performed in a STAR2000 HMDS/vapor prime oven from IMTEC. A 1.5 µm thick layer of AZ5214E photoresist from MicroChemicals was applied to the substrate using a SSE Maximus 804 cluster system and exposed in hard contact mode using a Karl Süss Mask Aligner MA6 (exposure wavelength 365 nm). The wafers were developed in AZ351 and exposed to $C_4F_8/SF_6/O_2$ plasma in a Deep Reactive Ion Etching (DRIE) Pegasus system from SPTS Technologies in order to create the patching capillaries (2 µm x 2 µm) for type A device. Alternatively, the wafer used to generate type B device was exposed to $SF_6/O_2/CHF_3$ plasma in a Reactive Ion Etching (RIE) system from SPTS Technologies. The wafers were oxidized for 40 minutes in a Tempress horizontal furnace at 1050 °C with an oxygen flow. After deposition of the thin oxide mask, a second lithographic step was performed. A layer of the same resist was applied and the wafer exposed in hard contact mode and developed. To etch the oxide, the wafers were exposed to a C_4F_8/H_2 plasma in an Advance Oxide Etching (AOE) from SPTS Technologies and then etched with a ramped Bosch process in a DRIE Pegasus system to create the deep channels in the silicon (200 µm wide, 50 µm deep). The fabrication was then completed by wet etching in a polysilicon etch mixture of HNO3, BHF and H2O in the ratio 20:1:20 for 8 minutes at room temperature to remove any defects and grass at the bottom of the deep channels. The remaining of the oxide mask was removed in a buffered HF solution. Smoothing of the sidewalls of the extracellular channel by thermal oxidation was performed in the horizontal furnace;

the wafers were oxidized for 150 minutes at 1100°C with an oxygen flow. The oxide layer was then stripped in a buffered HF solution. An additional layer of tetraethyl orthosilicate (TEOS) oxide was deposited in a low pressure chemical vapor deposition (LPCVD) furnace from Tempress at 725°C.

To prepare the samples for electroplating, a conductive gold and titanium seed layer was sputtered. Electroplating was then performed in an electrochemical bath, Microform 200 from Technotrans and gave nickel coverage with a thickness of about 300 µm. The silicon wafers were then dissolved in a KOH bath at 80°C. The resulting nickel plates were punched into 85 mm diameter shims by using a hydraulic press fitted with a customized punching tool.

Replicas of the original structures were injection molded with a Victory 80/45 Tech injection molding machine from Engel, with one of the nickel shims installed into the mold. A variotherm process was used with nozzle temperature of 280°C, mold temperature of 130°C and demolding temperature below 60°C. The holding pressure was 1700 bar and decreased to 0 bar in 0.75 seconds. Chips were molded from COC TOPAS grade 5013 (glass transition temperature, Tg of 135°C) from TOPAS Advanced Polymers GmbH. A 100 µm thick extruded polymer film TOPAS 5013F-04 from Advanced Polymers Extrusion Lab was used as a cover lid. Both the chips and the foil were exposed to UV radiation from a UV lamp (DYMAX mercury UV-bulb F/5000) emitting over the full unfiltered Hg line spectrum with a power of 44.5 W/cm^2 measured at the wavelength 365 nm, for 30 seconds and pressed together using a hydraulic press. In order to assure uniform pressure all over the chip surface, an aluminum holder was built in which the Luer fitting protrusions could be inserted. The holder was designed to accommodate 7 chips, so they could be bonded at the same time. In addition, a stack consisting of low roughness nickel disks and a thin PDMS gasket were positioned on top of the chips during bonding in order to preserve the transparency and to compensate possible non-uniformities in flatness. Sealing employed a piston force of 40 kN applied for 10 minutes, while maintaining a temperature of 115°C.

4. DEVELOPMENT OF THE POLYMER DEVICE

During the development of the polymer devices, we faced challenges due to the demolding of the polymer parts during the molding process. One of such challenges was the scratching of material from the sidewalls of the deep channels during demolding. In the worst case, the scratched material blocked the orifices and made the devices useless. Therefore, several types of etching and masking methods for the origination of the silicon masters were investigated, and Figure S4 shows micrographs of the Y shaped shallow channel in different phases of the development. In the beginning the fabrication process enrolled a standard Bosch process for the deep channels and the resulting polymer parts showed scratches of material that blocked the apertures (Figure S4A). We then performed the etching experiments with a continuous etching process to taper the sidewalls for easy demolding and the etching of the shallow channels was postponed to the end of the process by using a thick oxide layer as mask. The orifices were successfully replicated but defects were reported at the bottom of the shallow channels due to the very long etching times required, see Figure S4B. Therefore we employed a thinner oxide layer and optimized the molding process and accurate replication was achieved (Figure S4C). A device for capturing of single cells with 4 μm deep apertures originated from those polymer chips Tanzi *et al.*[3] To achieve smaller and in particular shallower (2 μm) apertures needed for patch clamping, the process was modified as presented in Table 1. Photoresist was chosen for masking and a thin layer of oxide was applied after the first etching step to avoid damages at the bottom of the patching capillaries during the rest of the process. At the same time, a ramped Bosch etching process was used for the deep channels. Moreover alternation of wet etching steps and oxidations was employed in order to smooth the surfaces around the patching holes (Figure S4D).

5. FIGURES AND TABLE

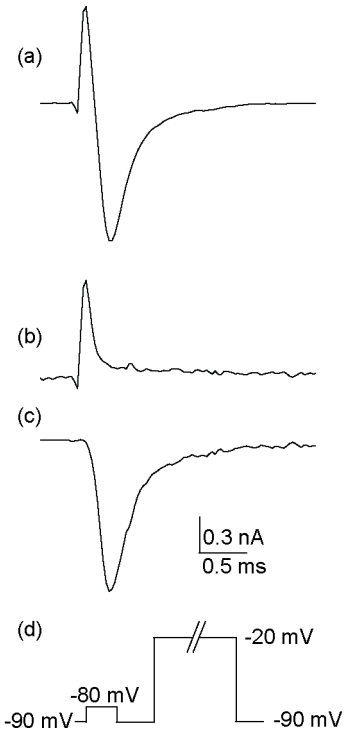

Figure S1. Leakage current subtraction using leak subtraction method. A) Whole-cell current recorded in response to voltage step from -90 mV (holding potential) to -20 mV. B) Leak current record produced by 10 mV test pulse multiplied by ratio between the two stimuli (70 mV/ 10 mV). C) Subtracted response of B from A in order to eliminate capacitive current. D) Voltage protocol.

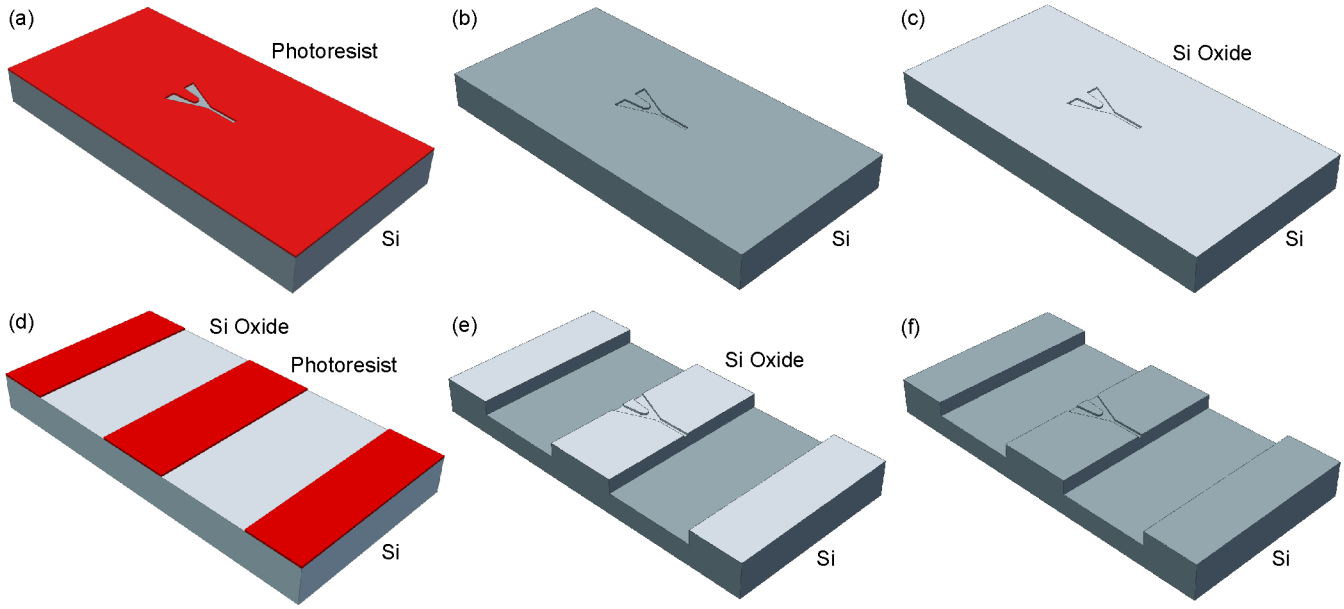

Figure S2. Schematics of the fabrication process for shaping the silicon after main steps: photolithography (a); silicon etching of the shallow patching channel (b); oxidation with 50 nm thick thermal silicon oxide (c); photolithography for the deep channel (d); oxide and silicon etching of the deep channels (e); oxide removal of the oxide mask (f).

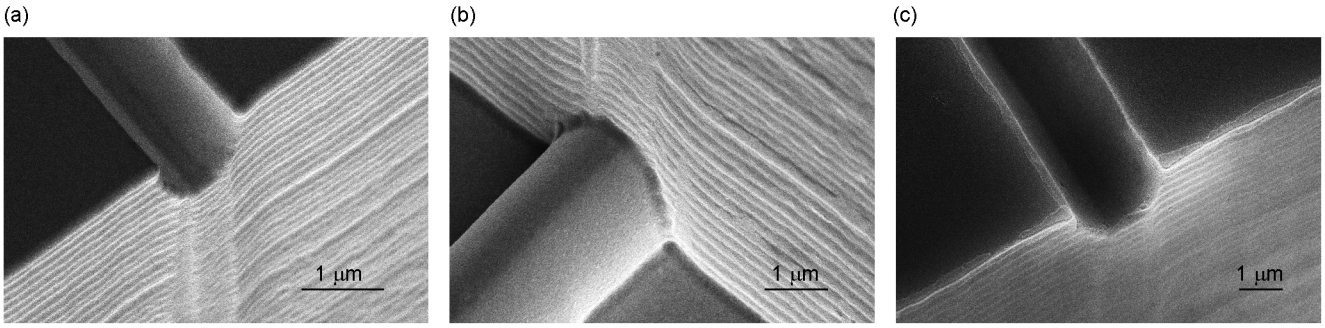

Figure S3. (a-c) SEM micrographs of the patching orifice after the main three steps of the fabrication process for the sample type B: silicon master, nickel insert, and replicated polymer part (from left to the right).

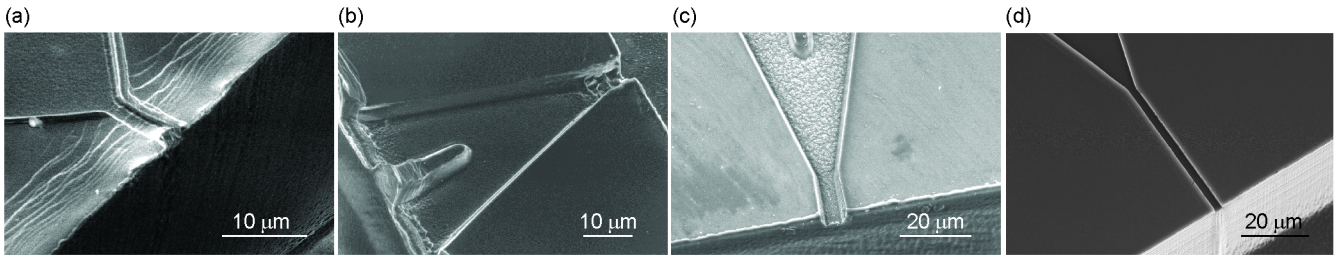

Figure S4. SEM micrographs of the capturing channel in the molded polymer chip. (a) In the beginning the orifice was blocked by accumulation of material during the demolding. (b) A circa 5 um wide patching channel was successfully molded but many defects were present. (c) Tapered sidewalls in the deep channel gave a replica with no defects. (d) Device molded with the presented fabrication process.

Process	***Parameters***
Oxide removal	HF bath ; t = 60 sec
Spin coating	- 1.5 µm AZ5214E - pre-bake: 90 °C for 90 sec
Photolithography	- hard contact mode, front side alignment W/A= 7 mW/cm2 ; t = 6,7 sec - AZ351 developer; t = 63 sec
Device type A *Si DRIE* *(shallow channels)*	C4F8/SF6/O2 = 150/275/5 sccm; 11 cycles; t = 24.2 sec
Device type B *Si RIE* *(shallow channels)*	SF6/O2/CHF3 = 30/29/5 sccm; t = 24 min; WRF = 20 W; P = 80 mTorr
Wafer cleaning	RCA 1:H2O:NH4OH:H2O2 (5:1:1); RCA 2:H2O:HCl:H2O2 (5:1:1) HF bath
Oxide deposition	1050°C dry oxidation ; t = 40 min + 20 min annealing
Spin coating	- HMDS vapor deposition - 2,2 µm AZ5214E - pre-bake: 90 °C for 90 sec
Photolithography	- hard contact mode, front side alignment W/A= 7 mW/cm2 ; t = 8 sec - AZ351 developer; t = 70 sec
Oxide etch AOE *(deep channels)*	C4F8/H2 = 5/4 sccm; t = 25 s; WRF = 200 W; T = 0°C; P = 4 mTorr
Si DRIE *(deep channels)*	C4F8/SF6/O2 = 150/275/5 sccm; 215 cycles; t = 552 sec
Polysilicon etch	H2O:HNO3:BHF (20:20:1); t= 8 min; T= 20°C
Oxide removal	BHF bath; t = 3 min
Wafer cleaning	RCA 1:H2O:NH4OH:H2O2 (5:1:1); RCA 2:H2O:HCl:H2O2 (5:1:1) HF bath
Oxide deposition	1100°C dry oxidation ; t = 150 min + 20 min annealing
Oxide removal	HF bath; t = 15 min
TEOS deposition	T = 725°C; t = 17 min; P = 190 mTorr; TEOS/O2 = 50/30 sccm

Table S1. The Table shows the process parameters for origination of the silicon master

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2 Sontheimer, Harald,Olsen,Michelle L., in , ed. ed. Wolfgang Walz, Humana Press, Totowa, New Jersey, 2007, pp.35-68.

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