Supporting Information to:

High-performance Top-gated Monolayer SnS$_2$ Field-effect Transistors and Their Integrated Logic Circuits

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**Figure S1.** Micro-photoluminescence of single layer SnS$_2$ flake fabricated for TG-FET.

**Figure S2.** Powder XRD of SnS$_2$ bulks, red lines denote from the standard card and the white peaks correspond to XRD data. The exfoliated source demonstrates pure hexagonal SnS$_2$ with JCPDS NO.83-1706.

**Fig. S3 (a,b)** AFM image of multiple layer SnS$_2$ flake and its height profile along the black line. The white dotted line shows the boundary of two neighbor layers and the height difference is ~0.7 nm. The 0.7 nm scanning demonstrate that our AFM instruments can identify monolayer scanning.
Figure S4. BG-FET performances with bare top surface, the carrier mobility is \(~10\ \text{cm}^2/\text{V}s\).

For the calculation to the BG-FET mobility: The BG-FET was measured in standard back-gated FET structure utilizing 285 nm SiO\(_2\) covering layer with bare SnS\(_2\) flake top surface as the channel. For the calculation of mobility, we utilize the linear working zone of FET as

\[ \mu_{BG} = \frac{g_m}{W C_i} \times \frac{1}{V_{DS}} \]

while the transconductance \( g_m = \frac{dI_{DS}}{dV_{BG}} \) was extracted from Fig. S2d, \( g_m = 8 \times 10^{-10} \ \text{A/V} \); the capacitance per unit area of SiO\(_2\), \( C_i = \varepsilon_0 \varepsilon_r / d = 8.85 \times 10^{-12} \ \text{F/m} \times 3.9 / (285 \times 10^{-9} \ \text{m}) = 1.21 \times 10^{-8} \ \text{F/cm}^2 \); The ratio of channel length to width is \(~5/3\). Substituting all the above data, we can get

\[ \mu_{BG} = \frac{g_m}{W C_i} \times \frac{1}{V_{DS}} = 8 \times 10^{-10} \times \frac{5}{3} \times \frac{1}{1.21 \times 10^{-8}} \times 100 \ \text{cm}^2/\text{V}s \]

\(~10\ \text{cm}^2/\text{V}s\).
Figure S5. Leakage current ($I_G$) stands in the order of $10^{-14} - 10^{-12}$ ampere during our measurement.