Electronic Supplementary Information

White light emission from heterojunction diodes based on surface-oxidized porous Si nanowire array and amorphous In-Ga-Zn-O capping

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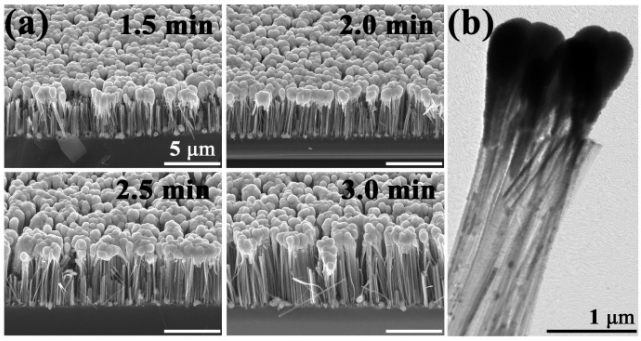

Figure S1. (a) SEM micrographs showing the morphology of the 'nanomatch' p-n heterojunction structures formed by depositing *a*-IGZO capping on the top end sides of the PSiNW array (scale bars indicate 5 μm). The 'chinks' near the SiNW root areas are Ag nanoparticles that functioned as catalysts during the electroless etching process; (b) TEM contrast image showing the detailed shape of the individual 'nanomatch' structure.

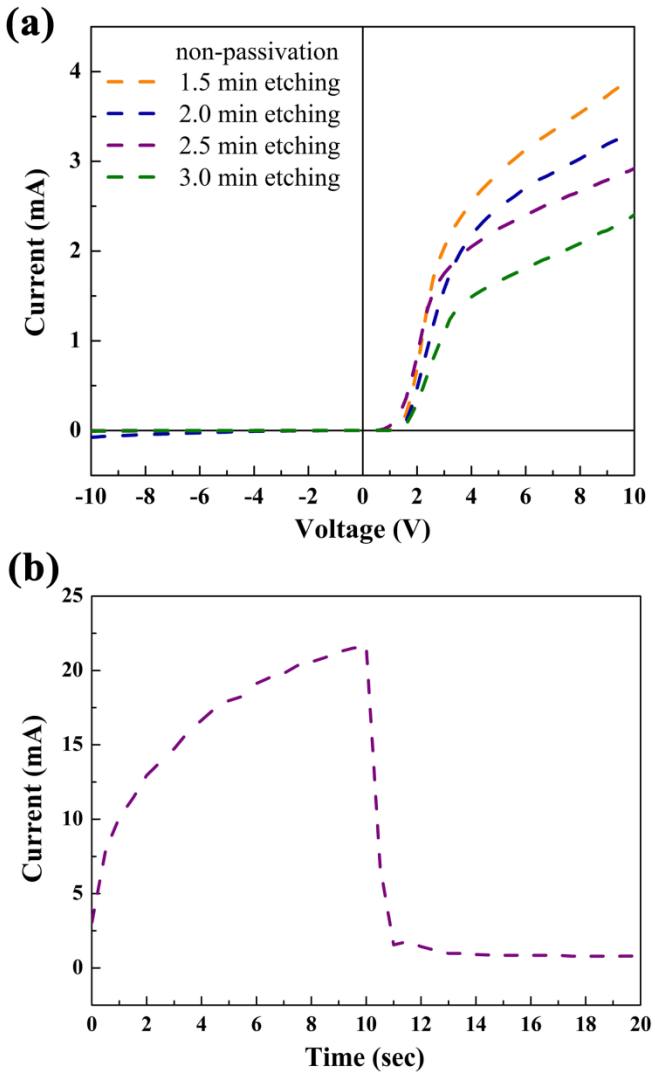

Figure S2. *I–V* characteristics of the control diode prepared using PSiNWs without surface oxidation. While the turn on voltage is much lower than that of the device prepared using surface-oxidized PSiNWs, the resistances (reciprocal of the first derivative of the *I–V* curve) increase abruptly at certain voltages. In addition, the device showed failure at the applied voltage above 10 V.

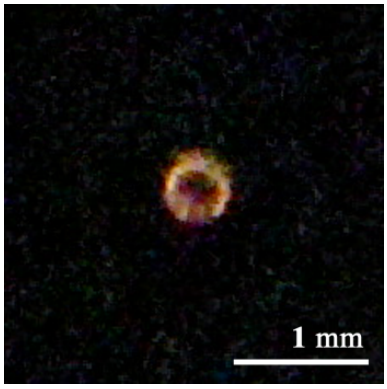

Figure S3. EL microscope image obtained from a control LED prepared with pristine PSiNWs showing pale orange light emission indicating the the absence of the green and blue emissions.

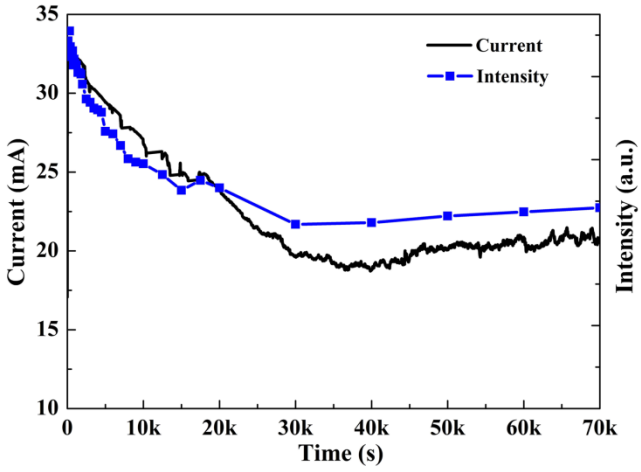

Figure S4. Tendency of light emission and current appraised for 20 hr at a fixed voltage of 15V.

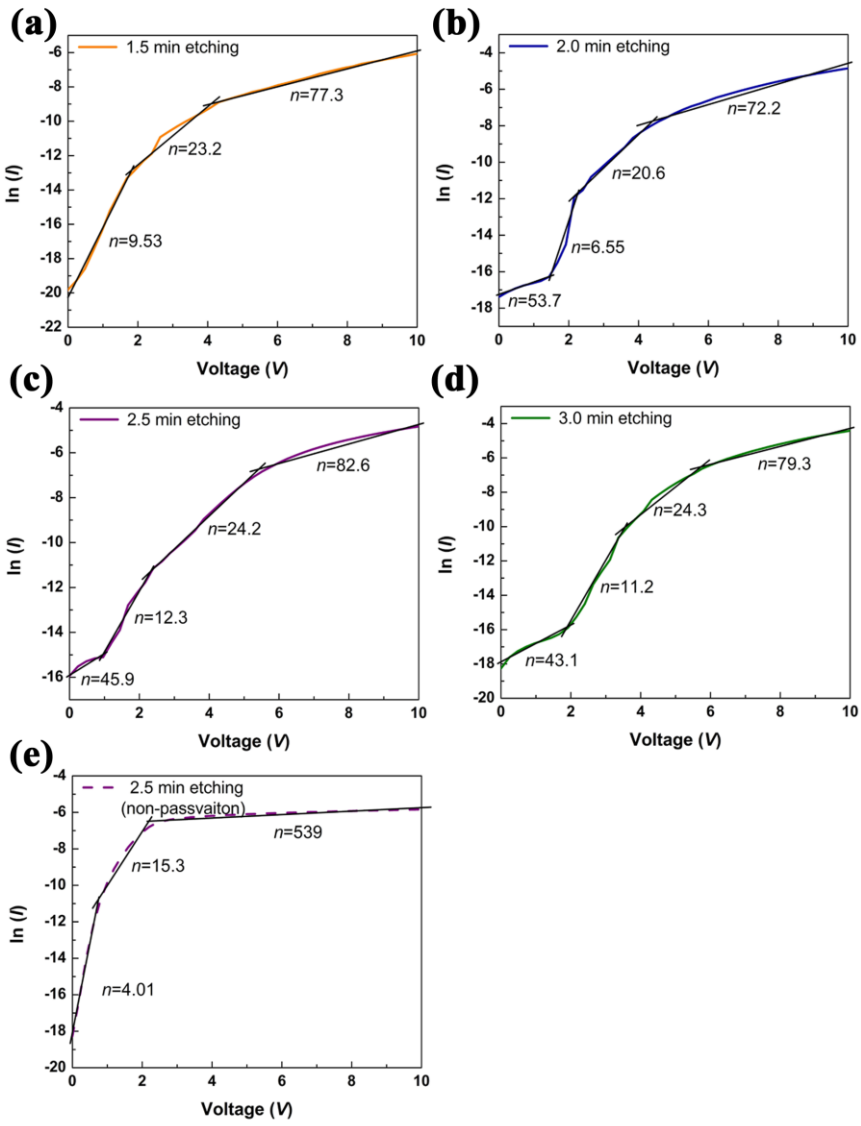

Figure S5. ln(*I*)–*V* characteristics of the PSiNW/a-IGZO device using the PSiNWs with ((a)–(d)) and without surface passivation (e). The ideality factors are much higher than 2 implying the presence of defect states in Si NWs although heterostructure diodes based on wide band gap materials have generally high ideality factors.[1–3] The changing ideality factors with varying applied voltage suggests that these devices have more than one recombination path of electrons and holes.[4] The ideality factor of device without passivation was extremely increased in high voltage regime due to the deep level trap from surface defects.[5]

References

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