Electronic Supplementary Material (ESI) for Nanoscale
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Vertical nanowire array-based field effect transistors for ultimate scaling

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This file includes:

Supplementary material S1

S1: Top surface topography of the low-k dielectric layer that covers the Si NW array using Atomic Force Microscopy (AFM).

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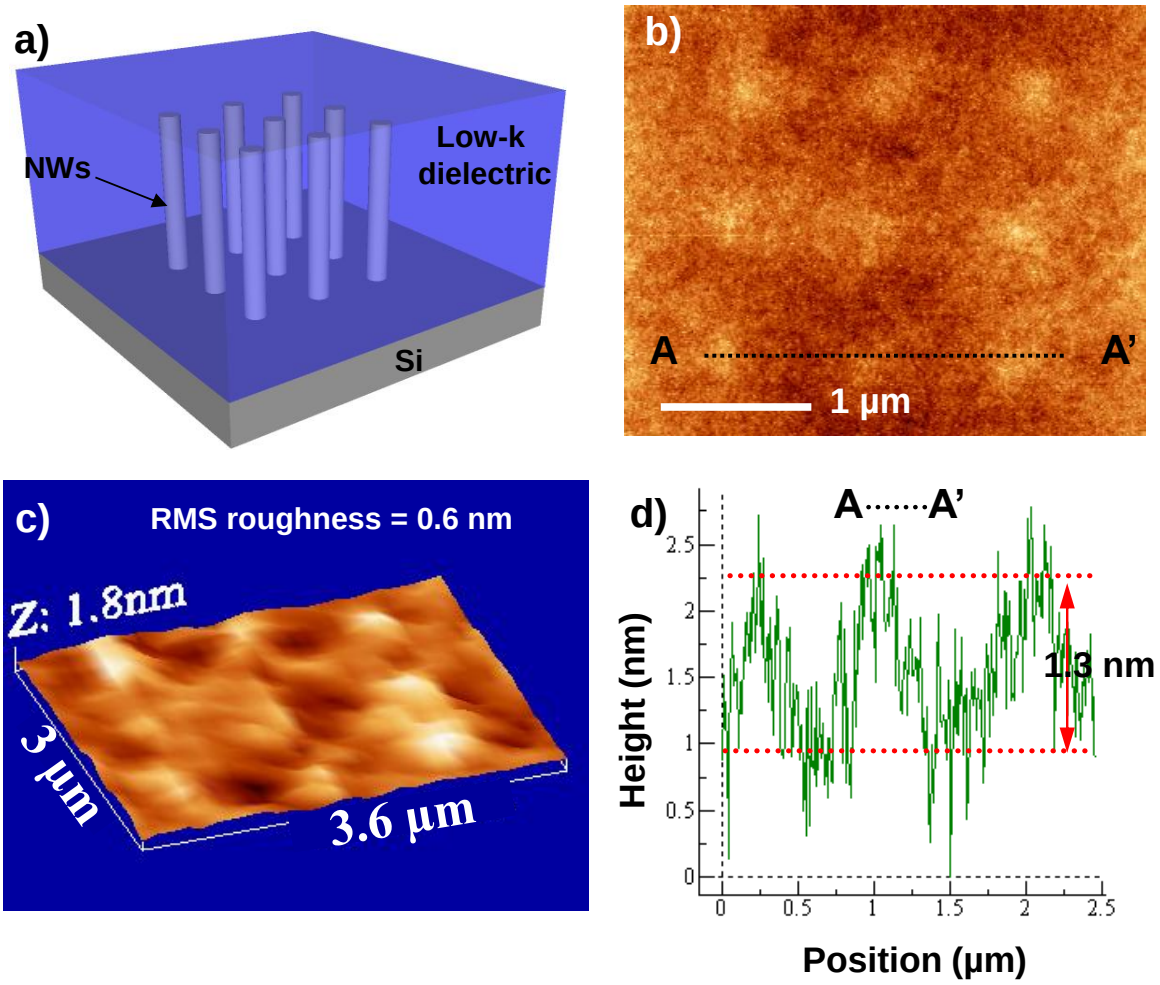

Supplementary Figure S1 (a) Schematic representation of vertical Si NW arrays (3 x 3) embedded in dielectric layer; (b-c) AFM images of dielectric top surface (320 nm thick) covering the vertical Si NWs arrays (3 x 3), 240 nm height; b) Two-dimensional (c) Three-dimensional image of low-k dielectric with an average 0.6 nm roughness; (d) A profile of the A - A' cross-line traced through three NWs in figure (b), the maximum height difference is approximately 1.3 nm. Images (b) and (c) correspond to 3 µm x 3.6 µm areas.