Supporting Information for

Graphene Nano-floating Gate Transistor Memory on Plastic

Sukjae Jang, Euyheon Hwang, and Jeong Ho Cho*

Figure S1. Magnified Memory hysteresis loop of the graphene NFGTMs based on various sizes of thermally-deposited Au NPs (cPVP thickness = 19 nm).

Figure S2. Retention time tests for the graphene NFGTMs based on cPVP tunneling dielectrics with thicknesses of 8 and 19 nm.