Electrodeposition as superior route to a thin film molecular semiconductor

Simon Dalgleish, a Hirofumi Yoshikawa, b Michio M. Matsushita, b Kunio Awaga b and Neil Robertson*a

a School of Chemistry and EaSTCHEM Research School, University of Edinburgh, West Mains Road, Edinburgh, UK. EH9 3JJ. Email: nrobert1@staffmail.ed.ac.uk
b Research Center of Materials Science, Nagoya University, Chikusa-ku, Nagoya 464-8602, Japan.

Supplementary Information

Supplementary figures

Fig S1: Scanning Electron Microscopy (SEM) images of solution deposited films of 1, formed by; (a) spin coating, and (b) drop coating; (c) pseudo drop coating.

Fig S2: Scanning electron microscopy (SEM) images of the initial stages of growth (< 1 minute at a potential $E = +0.5$ V vs. Ag/AgCl) for an electrodeposited film of 1 on an interdigitated platinum electrode array (electrode gap $L = 2 \, \mu m$).
Fig S3: FET characteristics of 1a measured for a FET device with channel length 2 μm and a SiO₂ layer thickness of 300 nm, showing change in IV characteristics by variation of V_{GS}.

<table>
<thead>
<tr>
<th>Electrolyte (initial dithiolene conc.)</th>
<th>Test 1</th>
<th>Test 2</th>
<th>Mean (weighted)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TBABF₄ (10 mM)</td>
<td>14.45(0.05)</td>
<td>13.2(0.2)</td>
<td>14.4(0.3)</td>
</tr>
<tr>
<td>TEABF₄ (10 mM)</td>
<td>1.564(0.004)</td>
<td>1.169(0.002)</td>
<td>1.2(0.2)</td>
</tr>
<tr>
<td>TEAPF₆ (10 mM)</td>
<td>7.04(0.02)</td>
<td>1.365(0.005)</td>
<td>2(2)</td>
</tr>
<tr>
<td>TBABF₄ (5 mM)</td>
<td>2.460(0.002)</td>
<td>2.295(0.003)</td>
<td>2.41(0.08)</td>
</tr>
<tr>
<td>TEABF₄ (5 mM)</td>
<td>3.4(0.2)</td>
<td>2.4(0.6)</td>
<td>3.3(0.3)</td>
</tr>
<tr>
<td>TEAPF₆ (5 mM)</td>
<td>4.50(0.08)</td>
<td>3.57(0.02)</td>
<td>3.6(0.3)</td>
</tr>
</tbody>
</table>

Table S1: Resistance measurements of deposited films with errors given.

The values of Test 1 and Test 2 are calculated as the mean of two measurements taken for each sample, with errors indicating the scattering of the results. Apart from TEABF₄ (5 mM), the errors are all below 2%, which indicates a high precision of measuring the conductivity in these samples. By calculating the weighted mean of the two separately prepared samples, one can see that the scattering of the values is dominating the error. With the exception of experiments TEABF₄ (10 mM) and TEAPF₆ (10 mM), the errors are below 10%, however the large errors especially in TEAPF₆ (10 mM) imply the need for further tests to be able to estimate the conductivity to an accuracy of more than the order of magnitude.
**Experimental**

Both 1 and [1][TBA] were prepared as previously described. Single crystals of 1 were grown by slow evaporation of DCM in the presence of 5% MeCN. The solvents used for electrodeposition, and solution deposition of 1, were purchased anhydrous from Wako pure chemicals or Sigma-Aldrich and used as received. All electrolytes for electrodeposition were purchased as electrochemical grade from Wako pure chemicals or Sigma-Aldrich, and dried under vacuum at 60°C prior to use.

Thin film X-ray diffraction was recorded on a Rigaku RINT2000 diffractometer (CuKα, λ = 0.15418 nm) at room temperature. Spectra were recorded on a sample width 0.02 cm, with beam width 0.5 mm, between 2θ = 5-50°, at a scan rate of 1.0°/min.

Scanning electron microscopy was performed using a Hitachi S-4300 electron microscope at 3 kV, giving a resolution of 5.0 nm, or better. Samples were visualised at working distance of 5.0 mm.

The resistance (R) of pressed pellet and single crystal samples were measured using a four-probe technique, attaching gold wires (diameter 25 μm) with a graphite paste. The resistance of the films was measured by a two-probe technique, connected directly to the interdigitated electrode arrays.

The FET devices comprised a silicon wafer and SiO₂ layer as the gate electrode and insulating layer, respectively. Platinum source and drain electrodes were deposited onto the insulating layer with an electrode gap of 2 μm. FET measurements were recorded on a HP probe station, measuring the drain current (I_DS) as a function of applied source drain voltage (V_DS) at various applied gate voltages (V_GS).

---