Electronic Supplementary Information (ESI)

Enhanced device performances of WSe$_2$/MoS$_2$ van der Waals junction p-n diode by fluoropolymer encapsulation

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Supplementary Information 1

Fig. S1 The current-voltage curves of two sets of WSe$_2$/MoS$_2$ heterojunction p-n diode on SiO$_2$/p$^+$-Si. (a) Pristine 1, 2, 3, and 4 diodes show non-ideal bad I-V properties, and (b) the pristine diodes (1,2) gets more degraded with Al$_2$O$_3$ showing higher reverse current.
Fig. S2 The current-voltage curves of another set of WSe$_2$/MoS$_2$ heterojunction p-n diode on SiO$_2$/p$^+$-Si. We performed this measurement to see the reproducibility of the effects of CYTOP encapsulation on property enhancement.
Supplementary Information 3

**Fig. S3** The current-voltage curves of another back gate (a) p-WSe$_2$ and (b) n-MoS$_2$ FETs on SiO$_2$/p$^+$-Si. We performed this measurement to see the reproducibility of the effects of CYTOP encapsulation on property enhancement (hole current increase in WSe$_2$ but electron current decrease in MoS$_2$ channel).
Fig. S4 Our p-n diode circuit in a schematic illustration (top) and an equivalent circuit diagram (bottom) where the parasitic capacitors ($C_1$ and $C_2$) are induced by the large overlapped area between electrodes (Pt, Ti) and heavily doped $p^+$-Si substrate. Thus these capacitors are connected parallel with our p-n diode and also connected with the external resistor in series. In the initial short moment of any fast switching, some displacement current can be caused through the $C_1$ and $C_2$ overriding the current through the diode. As a result, overshoot/undershoot behavior can be observed during the dynamics using $V_A=\pm5$ V.
Fig. S5 (a) Photo-induced I-V curves obtained from a pristine heterojunction p-n diode under R, G, and B LED lights. (The inset shows linear scale photo I-V curves in reverse bias regime.) Time dependent photocurrent responses (I-t) were also obtained at a reverse bias of $V_{IN}=-10$ V, at light pulse frequencies of (b) 2 Hz. Response time was ~more than 60 ms (even at -10 V), which is three times slower than that of CYTOP-encapsulated device. This may indicate that the junction or surface trap density in CYTOP-encapsulated diode is much lower than that of pristine device as we discussed in the main text with Fig. 5 and 6.
Supplementary Information 6

Fig. S6 Aging degradation of CYTOP-capped 2D p-n diode was not found for more than 8 days in air ambient of 40% relative humidity at room temperature, which indicates that our encapsulated diode is very stable in ambient.