

Supplemental figure 1:

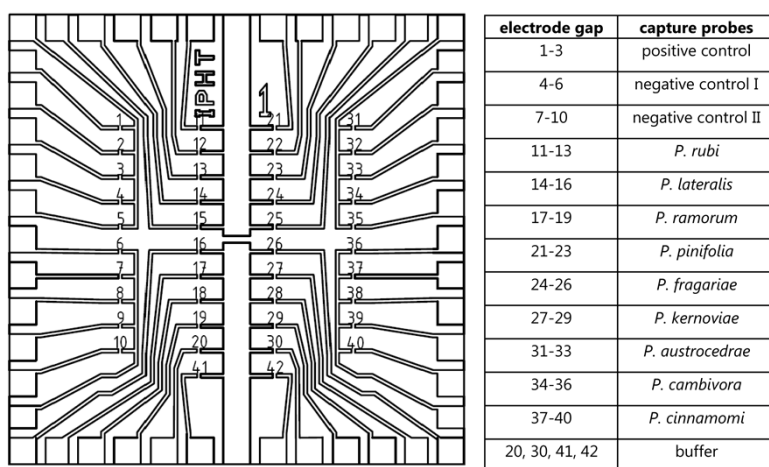


Figure S1: Spotting layout of capture probes on the chip.