

Supplementary Information

for

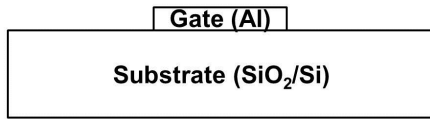
Surface grafting of octylamine onto poly(ethylene-*alt*-maleic anhydride) gate insulators for low-voltage DNTT thin-film transistors

Yun-Seo Choe,^{ab} Mi Hye Yi,^a Ji-Heung Kim,^b Yun Ho Kim,^{*a} and Kwang-Suk Jang^{*a}

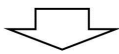
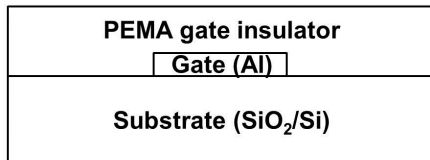
^a*Division of Advanced Materials, Korea Research Institute of Chemical Technology, Daejeon 34114, Republic of Korea. E-mail: kjang@kRICT.re.kr, yunho@kRICT.re.kr*

^b*School of Chemical Engineering, Sungkyunkwan University, Suwon 16419, Republic of Korea*

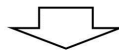
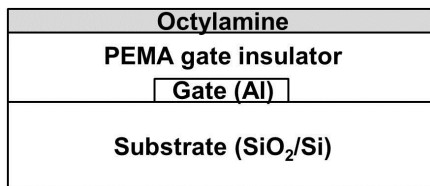
1) Al deposition using thermal evaporation



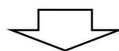
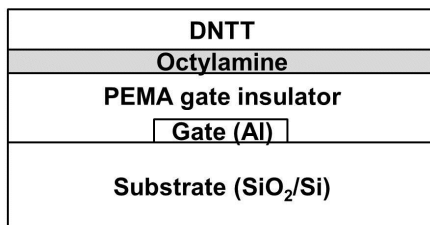
2) Spin-coating of PEMA gate insulator



3) Octylamine treatment by spin-coating



4) DNTT deposition using thermal evaporation



5) DNTT deposition using thermal evaporation

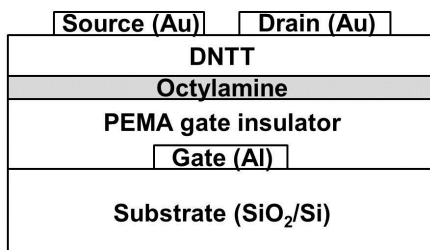
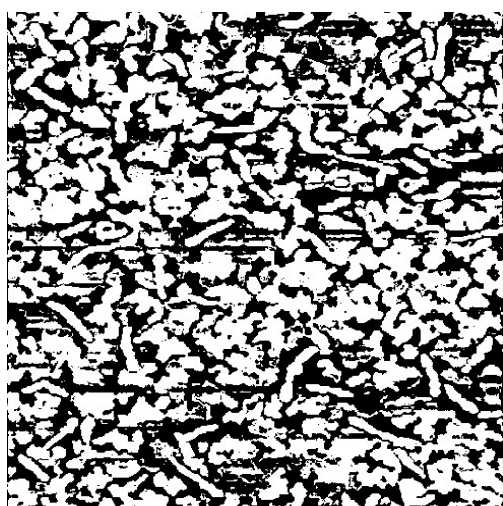
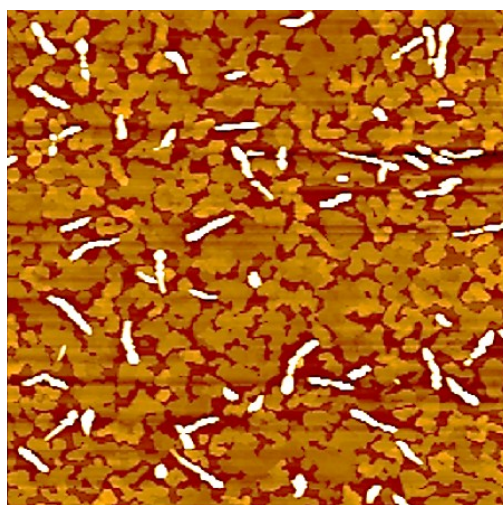


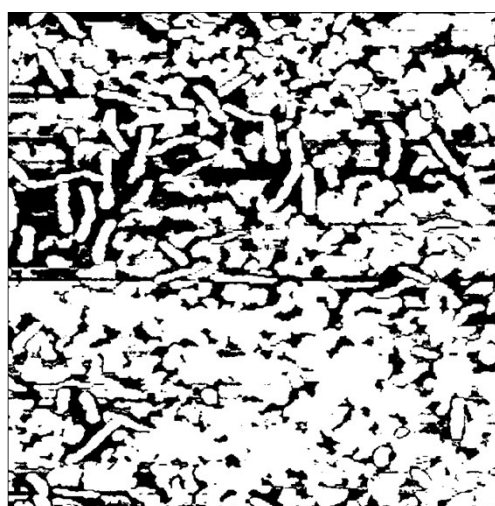
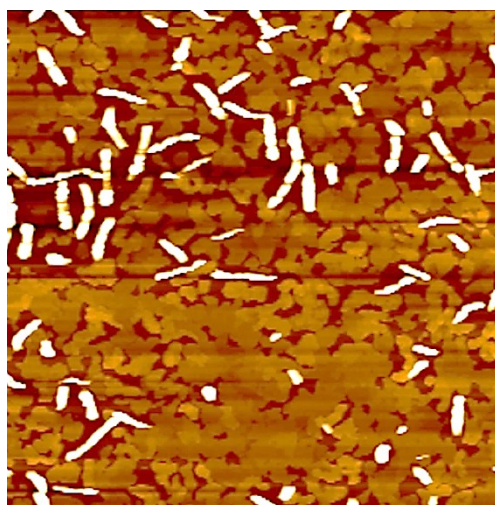
Fig. S1 Scheme of the TFT device fabrication.

non-treated



$$\rightarrow 100 - 49.544 = 50.467 \mu\text{m}^2$$

octylamine-treated



$$\rightarrow 100 - 30.711 = 69.289 \mu\text{m}^2$$

	Area	Mean	Min	Max	MinThr	MaxThr
1	49.533	255	255	255	9	255
2	30.711	255	255	255	255	255

Fig. S2 The surface coverage measurement of the 12 nm-thick DNTT layers on non-treated and octylamine-treated PEMA thin films.

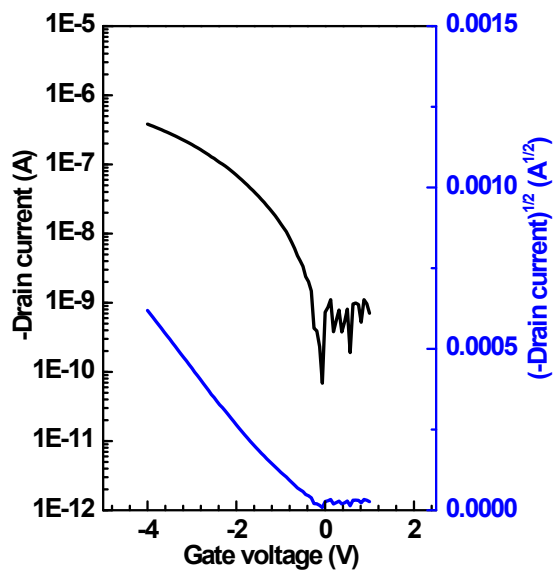


Fig. S3 Transfer characteristic (I_{ds} vs. V_{gs}) of the DNTT TFTs with the 60 nm-thick SiO_2 gate insulator.