

Sunlight-activated graphene-heterostructure transparent cathodes: enabling high-performance *n*-graphene/*p*-Si Schottky junction photovoltaics

Supporting information

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1. Tunable absorption of TiOx with different O/Ti ratio

TiOx was synthesized via sol-gel procedures as follow according to our previous article.¹ In brief, 2-methoxyethanol (CH₃OCH₂CH₂OH, Acros, 99+%) and ethanolamine (H₂NCH₂CH₂OH, Acros, 99%) were first mixed in a three-necked flask and titanium (IV) isopropoxide (Ti[OCH(CH₃)₂]₄, Acros, 98+%) was then injected after stirring for 10 min. The temperature was then raised to 80 °C and kept for 2 hours, followed by heating to 120 °C for 1 hour. The degree of hydrolysis was manipulated by the reaction atmosphere. With more oxygen and water concentration, the higher degree of hydrolysis would be

achieved. The TiO_x films consisting of different O/Ti ratios resulted in various band gaps and absorption spectra as shown in Fig. S1. In this work, we chose the TiO_x with a high O/Ti ratio ($x=1.9$) to ensure the spectral overlap between the absorption spectrum of TiO_x and the solar irradiation spectrum. The original concentration of as-synthesized TiO_x gel was 125 mg/mL. The precursor solutions with various concentrations were prepared by mixing with *n*-butanol (CH₃CH₂CH₂CH₂OH, Acros, 99%) to form the diluted solutions. The concentration of TiO_x used in this work for fabricating the graphene/TiO_x heterostructure thin films was 20mg/mL.

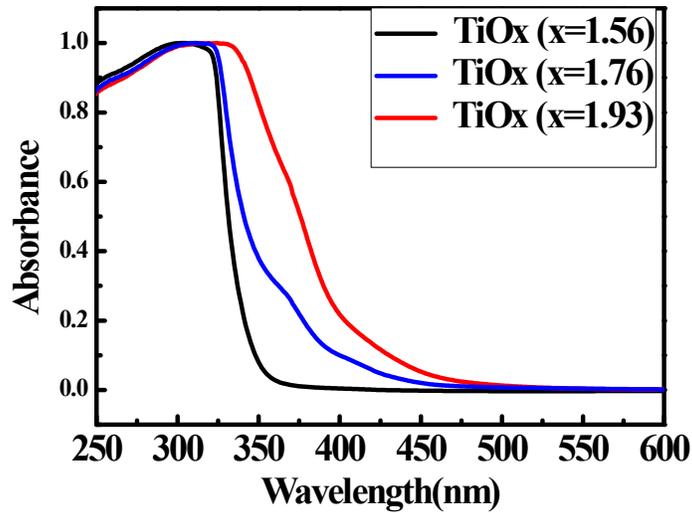


Fig. S1 UV-VIS absorption spectra of different O/Ti ratio of TiO_x.

2. Recovery process of the photoinduced doping effect

Fig. S2 shows the time-dependent source-drain current of the device under a pulse UV illumination covered with a 20 nm TiO_x thin film (top configuration) under light illumination in ambient condition. The transistor device subjected to photoinduced

doping had a gradual increase at drain current with illumination as a result of increased carrier concentrations. After the illuminated light was switched off, it exhibited a long recovery time because of the trapped charges.²

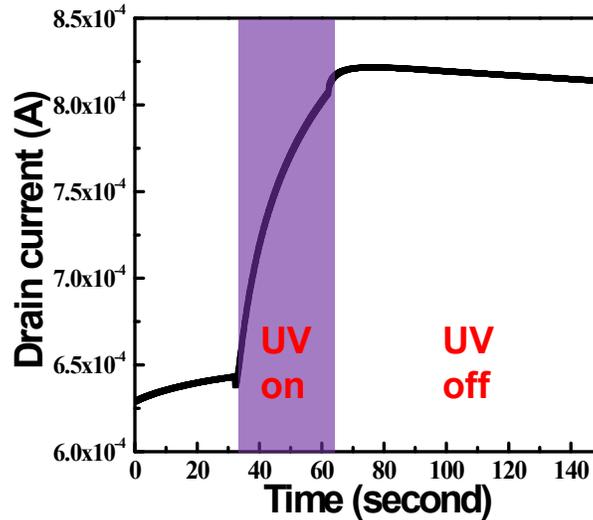


Fig. S2 Time-dependent source-drain current of the device under a pulse UV illumination.

3. graphene/*n*-Si v.s. graphene/*p*-Si (effect of native oxide)

Both *n*-type and *p*-type silicon wafers (1~10Ωcm) with 300 nm thermal oxide were used in this work. The major process for fabricating graphene/*n*-Si is similar to graphene/*p*-Si described in section 3. The only difference between these two devices is the backside electrode. In order to achieve ohmic contacts for *n*-Si and *p*-Si, we evaporated aluminum and gold for each device, respectively. The device structures of as-fabricated graphene/*n*-Si and graphene/*p*-Si is shown in Fig. S3 (a).

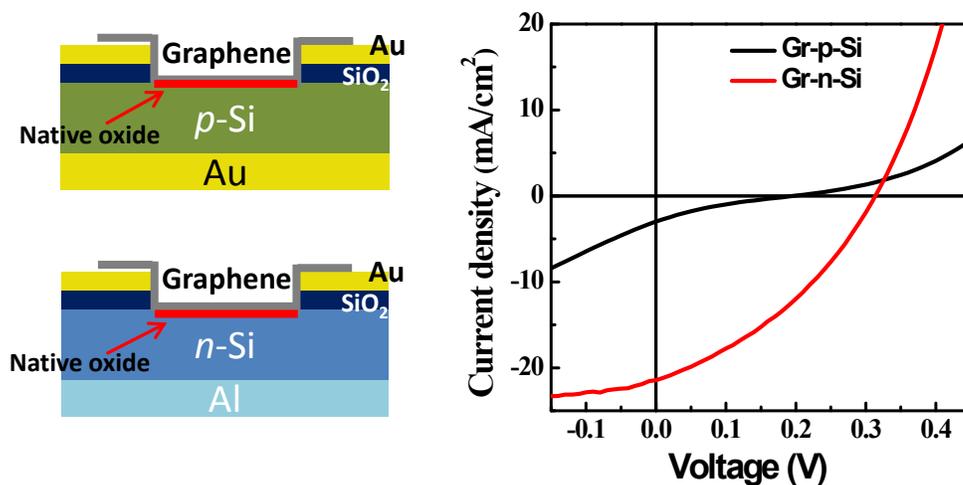


Fig. S3 (a) Schematic images of the graphene/*p*-Si (top) and graphene/*n*-Si (bottom) devices. (b) Performance of graphene/*n*-Si and graphene/*p*-Si Schottky solar cell without BOE treatment.

Typically, an as-transferred graphene/*n*-Si Schottky junction solar cell (where graphene acts as anode) demonstrates a much higher efficiency as compared to that of an as-transferred graphene/*p*-Si counterpart (where graphene acts as cathode). Fig. S3(b) shows the current-voltage curves of the two corresponding as-transferred graphene/Si Schottky junction solar cell. The power conversion of an as-transferred graphene/*n*-Si is 2.4%, whereas the power conversion of an as-transferred graphene/*p*-Si is 0.1%. The short circuit current of the graphene/*n*-Si device is seven times larger than the graphene/*p*-Si device. Although a native oxide layer is expected to form on both devices at the graphene/Si interfaces, the degradation of the device performance at the graphene/*p*-Si seems more severe than at the graphene/*n*-Si. This result may be explained according to the following model.

The interface between silicon and silicon oxide usually have a great amount of hole traps as mention in the previous MOS technique.^{3,4} As the devices are under illumination, the hole traps are filled with photo-excited carrier near the interface, either for *n*-type or *p*-type silicon devices, as shown in the top of Fig. S4. For a graphene/*n*-Si Schottky junction solar cell, the photo-excited holes at Si move toward graphene (Fig. S4 (a)). When hole traps at the graphene/*n*-Si interface are completely filled by the photo-excited holes from Si, the photogenerated holes near the graphene/*n*-Si interface can move toward the graphene more easily (Fig. S4 (b)). By contrast, for a graphene/*p*-Si Schottky junction solar cell, the photo-excited electrons at Si are expected to move toward graphene (Fig. S4 (c)). The electrons are expected to be recombined with the trapped holes at the interface when they move toward the graphene (Fig. S4 (d)). Once the trapped holes are recombined with photoexcited electrons near the interface, the trap states at the interface oxide will be further filled by the photo-excited holes near the interface. Therefore, more electrons will be recombined with the trapped holes again. Such a repeated process may cause the significant degradation in the device performance. This may account for the reason why a native thin oxide has a larger influence on the device performance of a graphene/*p*-Si Schottky solar cell than a graphene/*n*-Si counterpart.

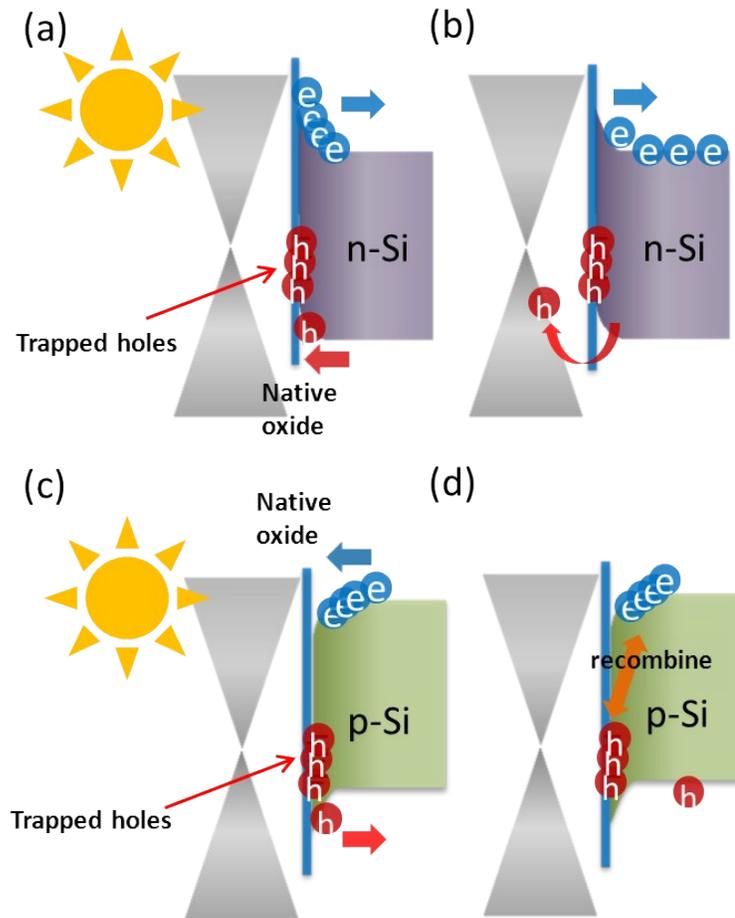


Fig. S4 Schematic representations of interfacial charge carrier transfer and recombination of at graphene/*n*-Si ((a) and (b)) and graphene/*p*-Si ((c) and (d)) Schottky junction interfaces.

Because the ultra-thin nature of native oxide $< 1\text{nm}$, we were not able to obtain the thickness of a native oxide when it was capped with graphene. However, we may trace the influence of growing native oxide on the device performance when the device was annealed at 150°C with various durations. The device showed a systematic degradation in the device performances of J_{sc} and FFs as the oxide layer was grown on Si surface under the 150°C annealing condition from 10 min to 30 min as shown in Fig. S5(a). In addition, we also showed the evolution of the aging effect on the device performance

when it was exposed in air up to 150 min, as shown in Fig. S5(b). Both results from Fig. S5(a) and (b) indicates that the formation of native oxide will degrade the device performances. Finally, we also compared the device performances with and without BOE treatment. As shown in Fig. S6(a) and (b) , if there is no BOE treatment, the device coated with the strong n-type dopant TiOx still showed a relatively low Jsc compared to that without coating the TiOx layer, indicating the importance of the BOE treatment for removing native oxide on the improvement of device performance.

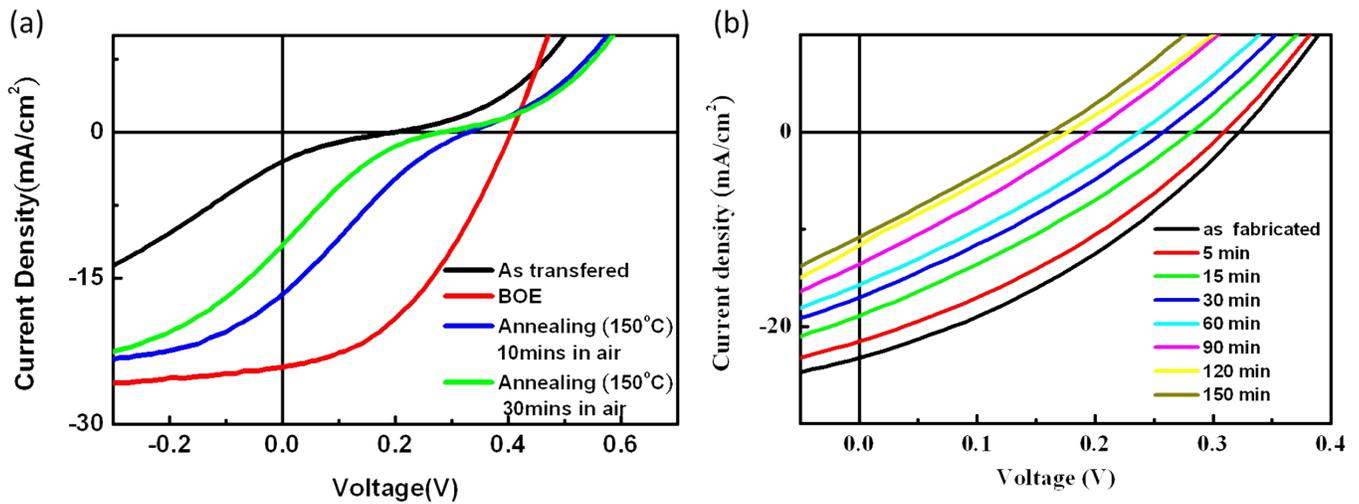


Fig. S5 Degradation of device performances with increased thickness of native oxide by thermal annealing 150°C in air (a) or when the device was exposed in air.

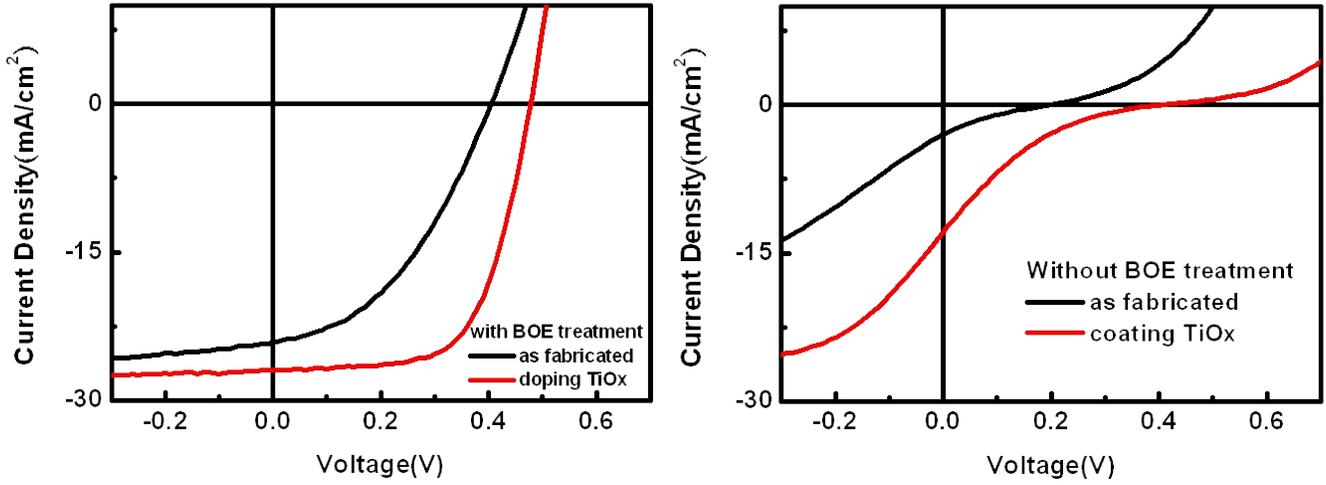


Fig. S6 Performances of devices with and without BOE treatment.

4. Increased Schottky barrier height of the photoactive TiOx/graphene

Deducing from the \ln J-V curve measured in the dark (Fig. S7), the current density exhibit adequate linearity over a range of three decades of J, and the extrapolation to zero bias yields the saturation current density J_s , which could be related to the Schottky barrier height based on the thermionic-emission diode equation:⁵

$$J(T,V) = J_s(T) \left[\exp\left(\frac{eV}{\eta K_B T}\right) - 1 \right] = A^* T^2 \exp\left(\frac{-e\Phi_{SBH}}{K_B T}\right) \left[\exp\left(\frac{eV}{\eta K_B T}\right) - 1 \right]. \quad \text{Where}$$

$J(T,V)$ is the current density across the graphene/p-Si interface, V is the applied voltage, T is the temperature and η is the ideal factor, A^* is the Richardson constant, and Φ_{SBH} is the schottky barrier height. Using the J_s values as describe before, the Schottky barrier height (SBH) values of the devices with pristine graphene and TiOx/graphene (no illumination) is 0.66V and 0.76V, respectively. Because there is a long recovery time at photo-active TiOx/graphene heterostructure as mentioned above, the dark current of the

photoactive TiOx/graphene/Si device was measured immediately when the illuminated light was switched off, where the Fermi-level of the TiOx/graphene is still quite similar to that when it was under illumination. The SBH of the photoactive TiOx/graphene/Si device was estimated to be 0.82V, as a result of a further increased work function of the photo-active TiOx/graphene transparent electrode, consistent with the observed increased open-circuit voltages of the devices.

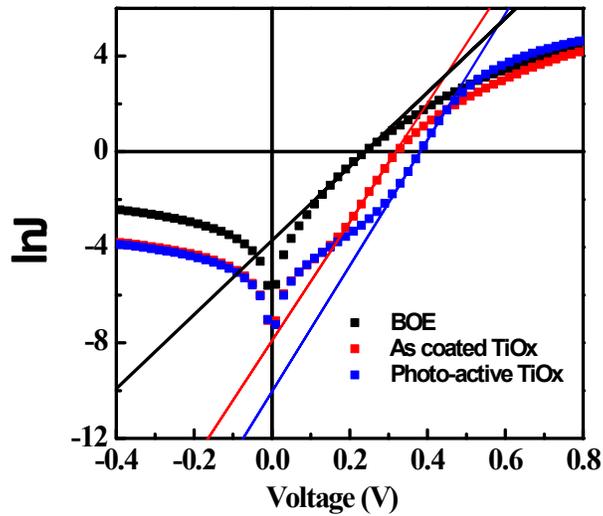


Fig. S7 Comparison of dark J-V curves for pristine, as-coated TiOx/graphene/*p*-Si (no illumination) and photo-active TiOx/graphene/*p*-Si (after illumination).

5. Antireflective technique with double layer coatings

The TiOx and PMMA could act as a double layer antireflective coating. Fig. S8 is the schematic image of double layer antireflective coating. The reflectivity is then calculated from the above parameters using the following formula based on Frenel equation:⁶

$$r_1 = \frac{n_0 - n_1}{n_0 + n_1} \quad r_2 = \frac{n_1 - n_2}{n_1 + n_2} \quad r_3 = \frac{n_2 - n_3}{n_2 + n_3} \quad \theta_1 = \frac{2\pi n_1 t_1}{\lambda} \quad \theta_2 = \frac{2\pi n_2 t_2}{\lambda}$$

$$R = |r_1^2| = \frac{r_1^2 + r_2^2 + r_3^2 + r_1^2 r_2^2 r_3^2 + 2r_1 r_2 (1 + r_3^2) \cos 2\theta_1 + 2r_2 r_3 (1 + r_1^2) \cos 2\theta_2 + 2r_1 r_3 \cos 2\theta_3}{1 + r_1^2 r_2^2 + r_1^2 r_3^2 + r_2^2 r_3^2 + 2r_1 r_2 (1 + r_3^2) \cos 2\theta_1 + 2r_2 r_3 (1 + r_1^2) \cos 2\theta_2 + 2r_1 r_3 \cos 2\theta_3}$$

The refractive indices of PMMA and TiOx⁷ are 1.49 and 1.68. Owing to the thickness of TiOx is about 20nm, the optimized PMMA thickness is about 70 nm to achieve a minimum reflection wavelength in the visible region (400~760nm).

Fig. S8 is the optical images of device before and after being coated with TiOx and PMMA. The uniform contrast in Fig. S8(b) shows that TiOx film covers the surface of graphene/Si. Fig. S8(c) shows the device after being coated with antireflective PMMA. The dark contrast of the device indicates that the PMMA/TiOx double layer noticeably reduces the reflection of light. The SEM cross-section image in Fig. S9 shows a uniform TiOx layer with thickness about 20nm when it was deposited on graphene/silicon. Although TiOx is a good encapsulated layer which may prevent the device from being exposed to oxygen and water, the thickness of TiOx is too thin to block all possible contamination in atmosphere. (also see Fig. 5(d) in the manuscript) Thus, a PMMA layer here not only acts as an antireflective layer but also acts as an additional encapsulated layer to further block the possible contamination of water or oxygen. Fig. 5(d) demonstrates the stability of devices covered with and without encapsulated layers of TiOx and PMMA.

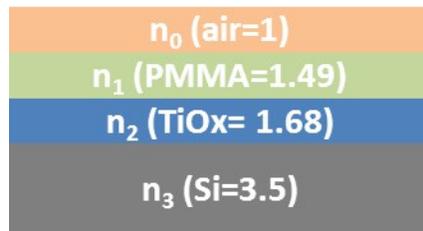


Fig. S7 Schematic representation of a double layer (TiOx and PMMA) antireflective coating

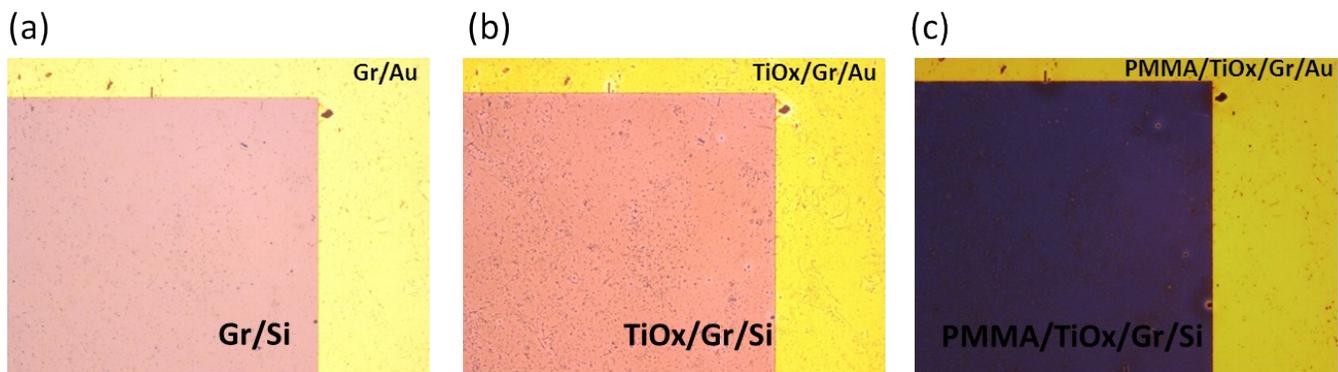


Fig. S8 Optical image of device before (a) and after being coated with (b) TiOx and (c) PMMA.

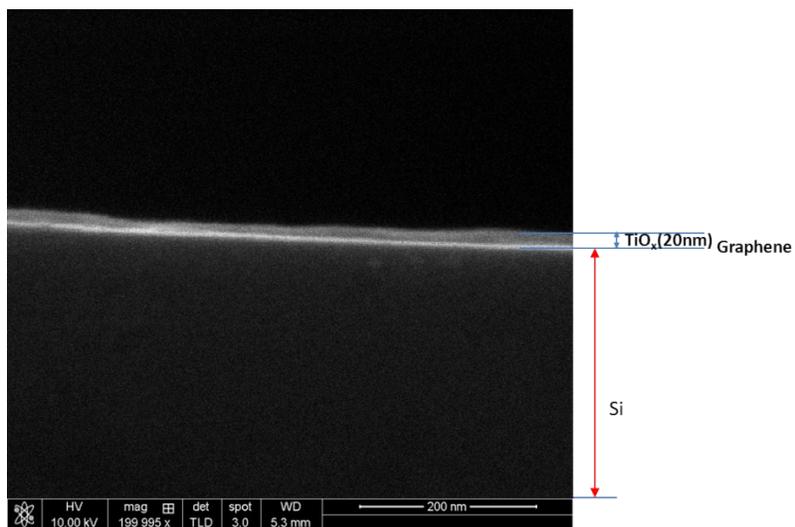


Fig. S9 SEM cross-section image of a TiOx/Gr/p-Si device

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