Electronic Supplementary Material (ESI) for Energy & Environmental Science.

Conductance and capacitance of bilayer protective oxides for silicon water splitting anodes

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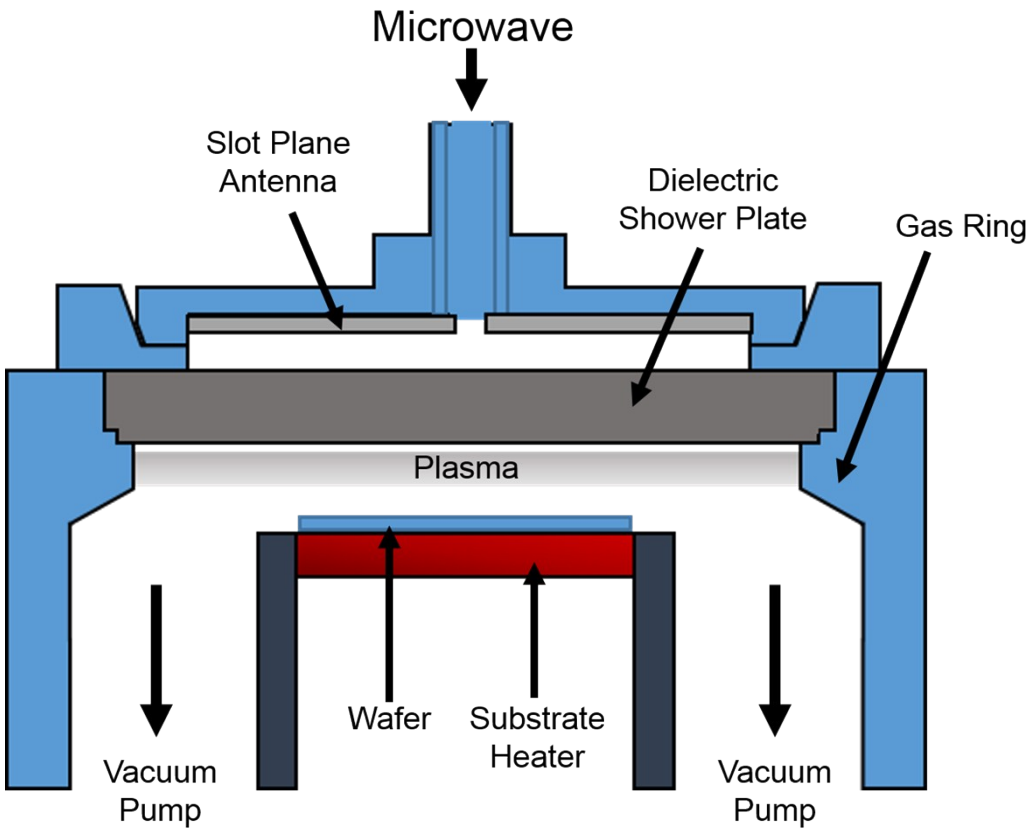
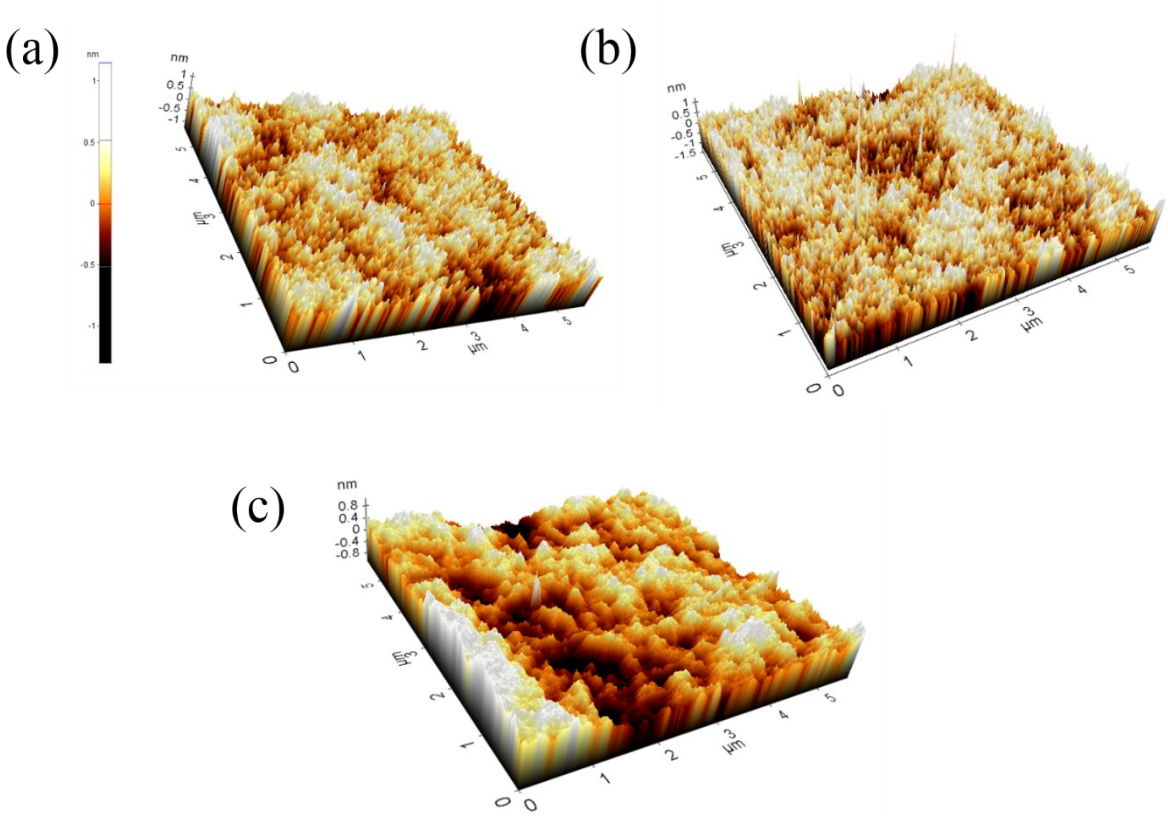
Supporting Information

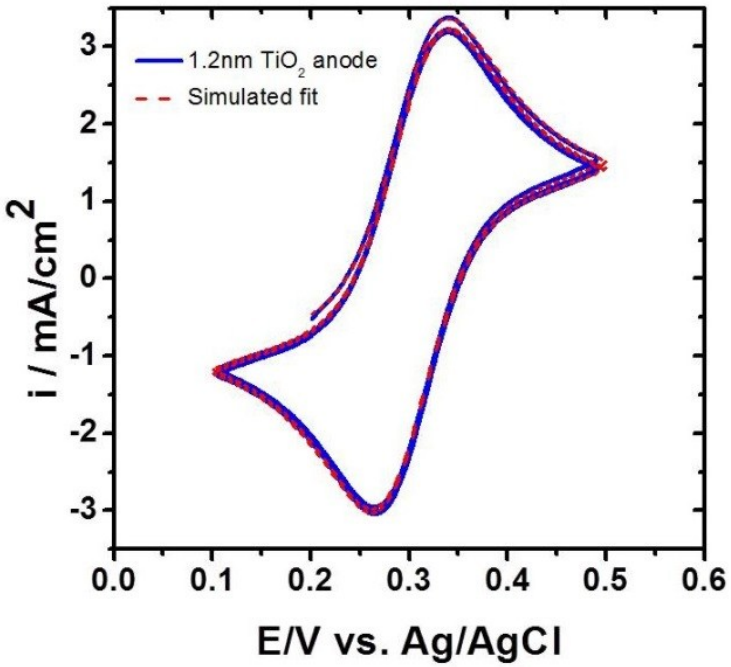


S1 | Schematic of the Slot-Plane-Antenna (SPA) reactor. These reactors are produced by Tokyo Electron Limited based on the earlier work of Ohmi et al. on Radial Line Slot Antenna (RLSA) [30]. SPA utilizes radical oxidation that can achieve ultrathin oxide layers with low D_{it} values and thickness reproducibility equal to or better than thermal oxidation, and at significantly lower temperatures--achieving 0.7 to 1.0 % thickness non-uniformity for films of 1.5 to 10 nm with D_{it} values below 10^{10} $eV^{-1}cm^{-2}$ at temperatures as low as 400˚C [31]. A 2.45 GHz microwave is introduced from the top of the apparatus and distributed across the slot plane antenna. As the microwaves are emitted downward they generate a uniform, high density plasma below the dielectric shower plate with a diameter exceeding 30 cm, capable of uniformly covering large wafers. Inert gases and oxygen are emitted through nozzles around

the gas ring and the substrate is heated resistively to temperatures between 400 ˚C and 500˚C for radical oxidation of ultrathin layers. For these experiments the deposition temperature was set to 500˚C, for an actual substrate temperature of approximately 400˚C and was allowed to equilibrate while argon was purged through the chamber at 100 sccm. Then the argon flow rate was increased to 1500 sccm and oxygen gas was introduced at 400 sccm for 10 seconds. Finally the argon flow was set to 1200 sccm and oxygen held at 40 sccm for 25 seconds at a process pressure of 5 Torr. The microwave power was set to 3000 W and held for the duration of the growth time (times in Table II below). After the microwave power is shut off, argon and nitrogen are allowed to flow for an additional 3 seconds to conclude the process. This process was optimized for the thinnest possible oxides; decreasing the process time to 3 - 5 seconds results in final oxide thickness of ~15 Å, the approximate minimum for this method. By extending the run length, oxide films of > 100 Å thickness can be grown; however, they require increasingly long deposition times.

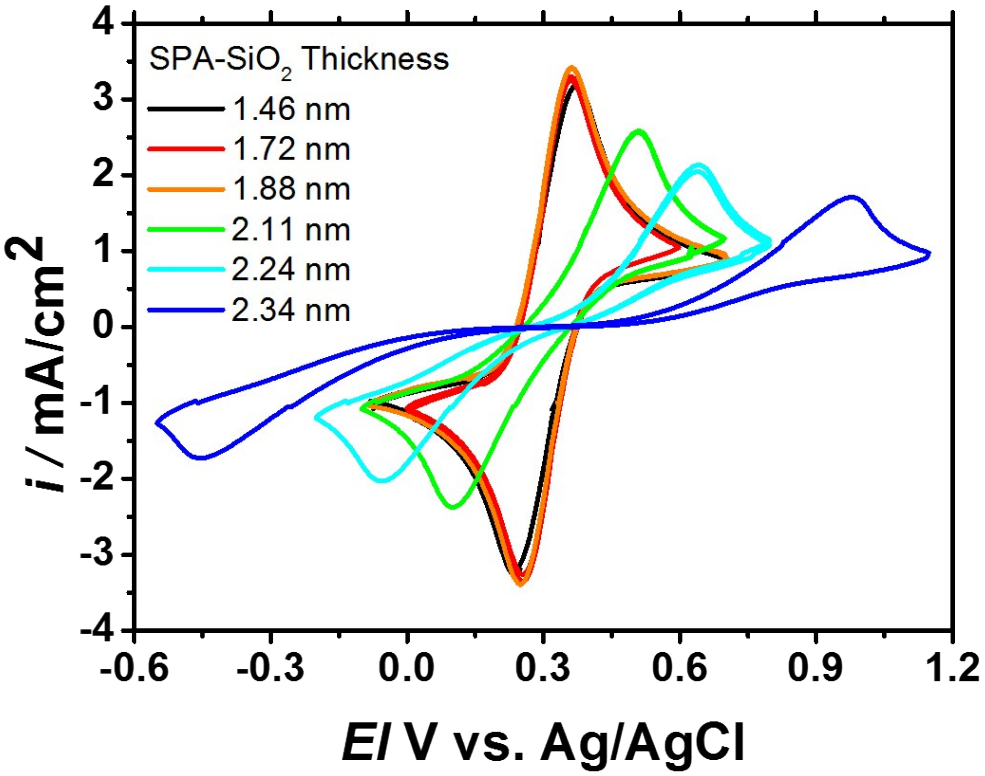


S2 | 3D Atomic force microscopy (AFM) renderings of the SPA-SiO_2 devices. AFM data is shown for three surfaces of interest: (a) 1.5 nm SPA-SiO_2 on silicon r_q = 0.276 nm (b) 2 nm Ir / 1.5 nm SPA-SiO_2 / Si r_q = 0.301 nm and (c) 2 nm Ir / 1.5 nm SPA-SiO_2 / Si after a 30 minute forming gas anneal at 450˚C r_q = 0.263 nm. The low rms roughness of all surfaces shows that the SiO_2 grows smoothly and uniformly, that the iridium also deposits smoothly on top as opposed to islanding, and that the iridium is able to stay intact during a 450˚C standard anneal. Studies have shown that the electron beam evaporated iridium does ball up at temperatures of 600˚C and above on a Si/SiO_2 surface. For all devices in this study, smooth and uniform surfaces are found.

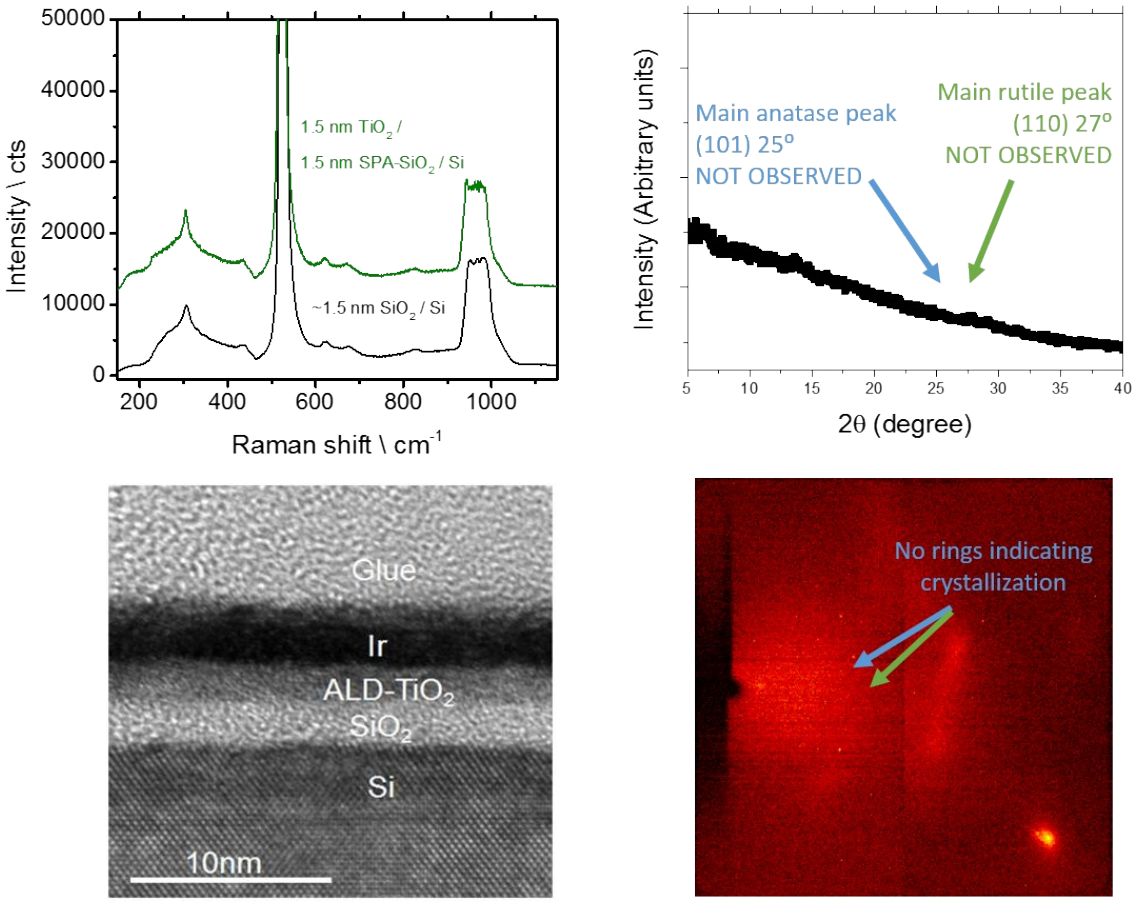


S3 | Simulated cyclic voltammograms for extracting the total resistance.

CV of (—) 2nm Ir/1.2nm TiO_2/1.5nm SiO_2/p+Si in FFC solution compared to (--) a simulated fit using EC-lab software. The cyclic voltammograms obtained in ferri/ferrocyanide were fit to theoretically determined profiles using EC-lab software V10.21. The high-frequency impedance determined series resistance of 18.4 Ω was first subtracted from all the data. The best performing anode close to approximately a Pt wire ideal reference was first fit assuming no uncompensated series resistance, a surface area of 0.196 cm^2, catholyte and anolyte concentrations of 10mM, a scan rate of 100mV/s, room temperature, and the charge transfer coefficient α=0.50. The best fit was obtained with E_0 =0.29 vs Ag/AgCl/sat. KCl electrode, k_0 = 0.01 cm/s, D_O = 8.5 x 10^{-6} cm^2/s, and D_R = 3.5 x 10^{-6} cm^2/s. Comparing these fitted parameters to literature: Daum and Enke find that the rate on an oxidized Pt electrode is 0.028, ten times less than the reduced surface [1]. It is not unreasonable to think a similar rate constant would apply to iridium oxide. Konopka and McDuffie studied the FFC redox couple also finding a higher diffusivity of the reduced species, in particular D_O=7.3 x 10^{-6} cm^2/s and D_R = 6.7 x 10^{-6} cm^2/s [2]. The voltammogram of each anode with increasing insulator thickness in ferri/ferrocyanide was then fit with the same parameters, only varying the uncompensated series resistance. The same procedure was followed for Si/SiO_2/Metal anodes as well as anodes with the TiO_2/SiO_2 and Al_2O_3/SiO_2 bilayers.

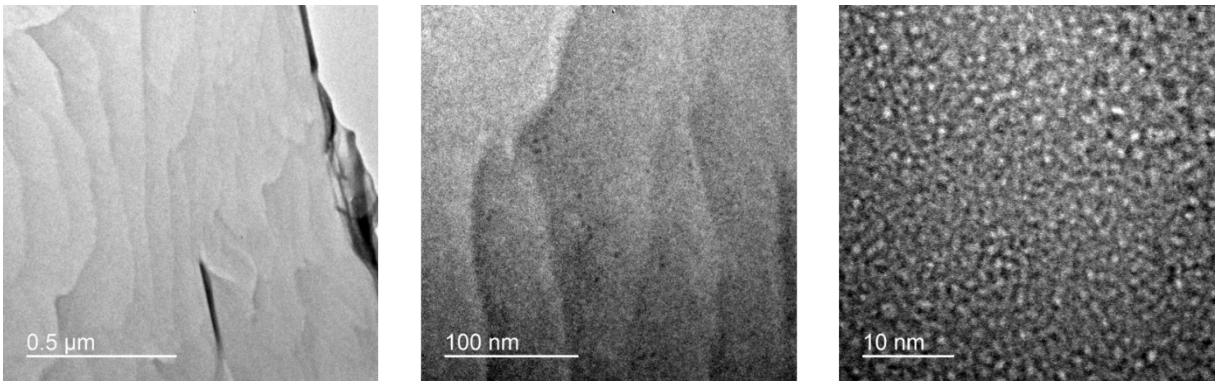


S4 | Electrochemistry data for Ir / 'x' nm SPA-SiO_2 / p^+Si anodes. Electrochemical results taken in the dark for 2 nm Ir / 'x' nm SPA-SiO_2 / p+Si. These CV are modelled to give the resistance results plotted in Figure 2 and 3 of the main manuscript revealing an exponential scaling that agrees well with the prediction of direct hole tunneling.

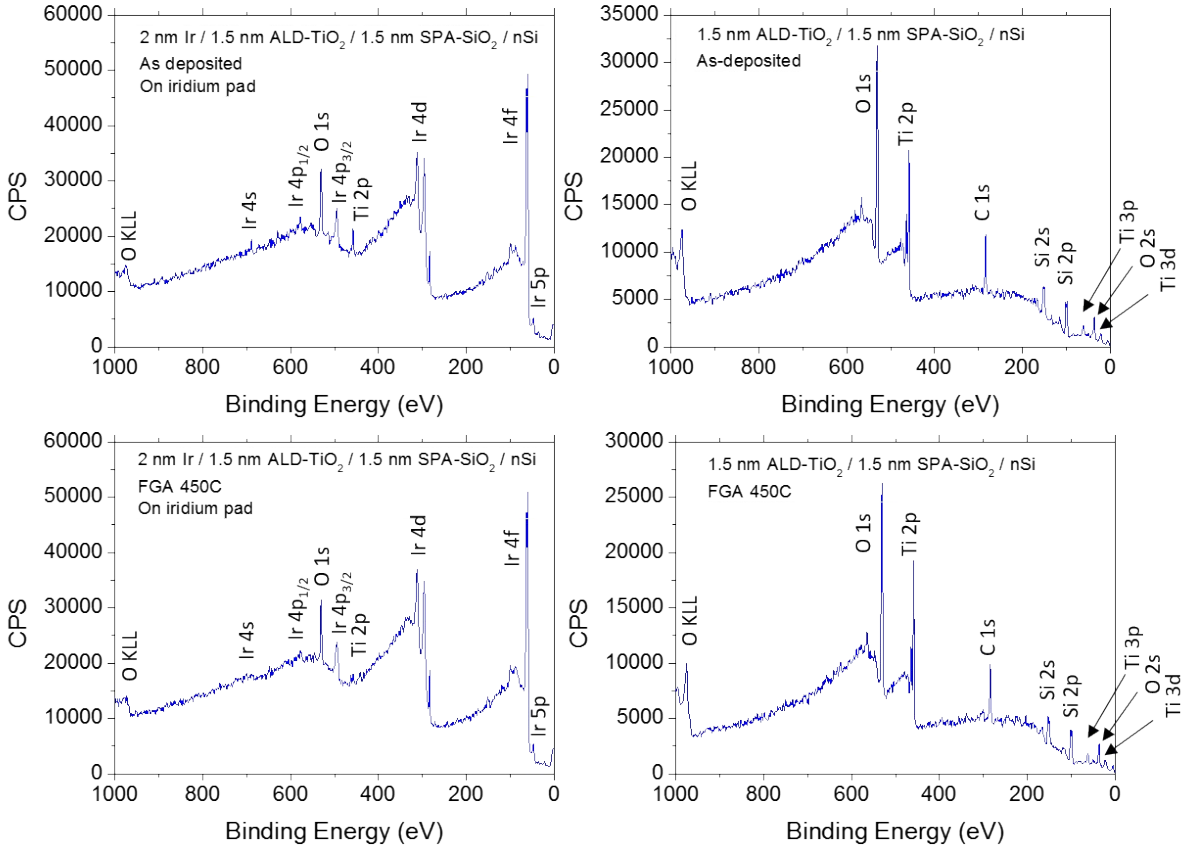


S5 | Raman, XRD, and TEM analysis showing the lack of crystallinity in the thin film layers after forming gas anneal at 450C. Ultrathin SiO_x interlayers are amorphous and the as-deposited ALD-TiO_2 was also shown to be amorphous previously [6]. In this study, similar films are studied as-deposited and after a 450°C forming gas anneal. Here physical characterization shows that the layers do not crystallize under these conditions. Because the film is ultrathin, the surface energy dominates and therefore crystallization does not occur at elevated temperature even though it would in the normal bulk material. Raman (top left) shows that the ALD-TiO_2/SPA-SiO_2 bilayer after a 450°C forming gas anneal gives the same signal as a bare silicon substrate. X-ray diffraction (XRD) (top and bottom right) show that no peaks occur at 25° or 27° where the highest intensity anatase and rutile peaks respectively would occur. Cross sectional TEM (bottom left) is also shown from reference 5. This is the exact same structure with a 450°C forming gas anneal, except that the ALD-TiO_2 is deposited on the vendor chemical oxide instead of the SPA-SiO_2. As shown in this study, the two produce identical results when of similar thickness. The TEM shows that the TiO_2 after FGA is conformal and still in the amorphous state. Other studies in the literature have also shown that ultrathin ALD-TiO_2 films on SiO_2/Si do not crystallize. A study by Mitchell et al. showed that

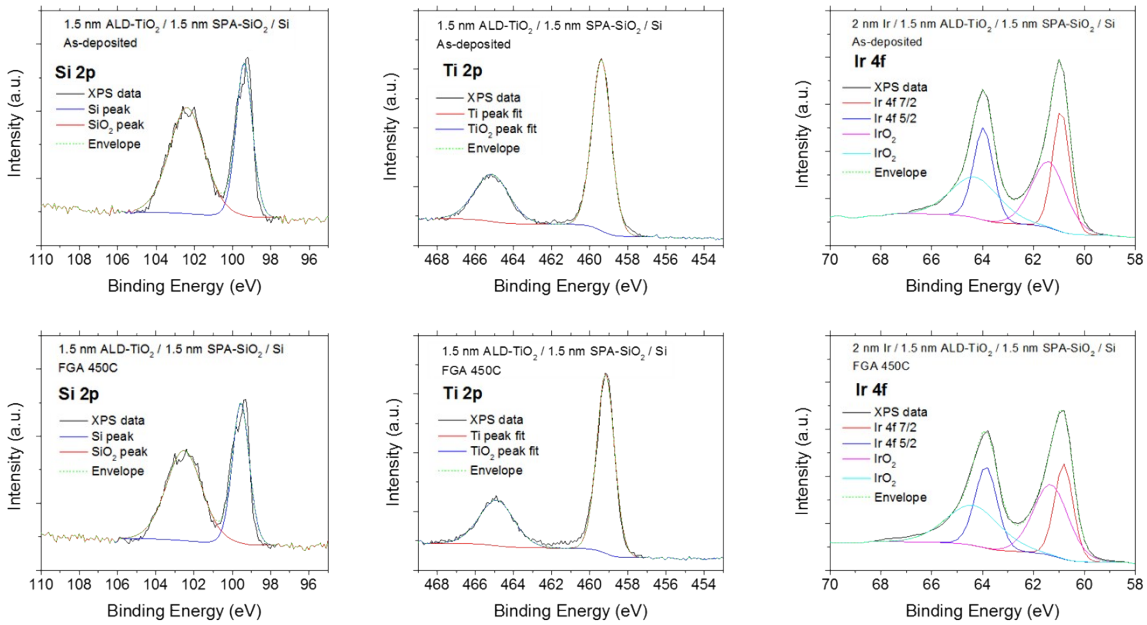
a 2.4 nm TiO_2 film remained amorphous after a 300°C deposition, whereas films of 8 nm and above successively showed more crystallization at the same conditions [3].



S6 | Plan view TEM analysis showing surface morphology and amorphous thin films. Plan-view TEM images at low resolution (left) and high resolution HRTEM (middle 100 nm, right 10 nm) show the morphology of the ALD-TiO_2 deposited on the SiO_x interlayer after a 450ºC forming gas anneal. The worm-like texture of the HRTEM image on the far right is characteristic of amorphous layers. No lattice fringes besides those of the underlying silicon substrate can be observed nor any diffraction patterns associated with anatase or rutile, similar to the XRD result shown in S5.



S7 | XPS survey scans of the Ir-coated (left) and bare (right) $TiO_2/SiO_2/Si$ stacks before and after the forming gas anneal. All expected peaks are observed and no contaminant peaks. When measuring on top of the 2 nm iridium, a small Ti 2p peak can be observed, but the underlying SiO_x and Si cannot due to the 3 – 5 nm escape depth of the photoelectrons. In the right images, when measuring on the bare TiO_2 surface, the SPA-SiO_2 and Si surface can be seen through the ALD-TiO_2. The surface composition and bonding is not significantly changed after the forming gas anneal.



S8 | XPS high resolution scans of Si 2p, Ti 2p, and Ir 4f regions. All regions are scanned before and after the forming gas anneal. Peaks are fit using a Shirley background. For the Si 2p peak, the ratio of the SiO_2 to Si peak goes from 1.48 to 1.35 after forming gas anneal, suggesting that the interlayer may be slightly thinned. The Ti 2p spectra is unchanged by the forming gas anneal. The Ir 4f spectra requires Ir^{4+} contributions to fit the spectra representing the presence of the IrO_2 even before electrochemical stressing. After forming gas anneal, slightly more of the Ir^{4+} species is present.

S9 | Ideal capacitance voltage behavior. Capacitance voltage (CV) analysis is a widely used technique to characterize metal-insulator-semiconductor gate stacks giving information about work functions, built-in field, dielectric constant, insulator thickness, interface and fixed charges, interface traps, and inversion behavior, all of which are important in MIS solar cells and MOS transistor gates among other devices. The overall opposition of a circuit to current with an applied voltage is referred to impedance where the real component is resistance and the imaginary is reactance. Reactance is due to two components: inductance, a built-up magnetic field which resists the change in current, and capacitance, a built-up electric field which resists the change in voltage. Static capacitance is defined as the charge stored per unit voltage, but the differential capacitance is typically measured, which is the ratio of the current and voltage time dependence. By measuring differential capacitance, we can study the charge stored in these MIS structures as well as the charge transferred by measuring the leakage helping complete the whole picture of operation for these leaky MIS structures.

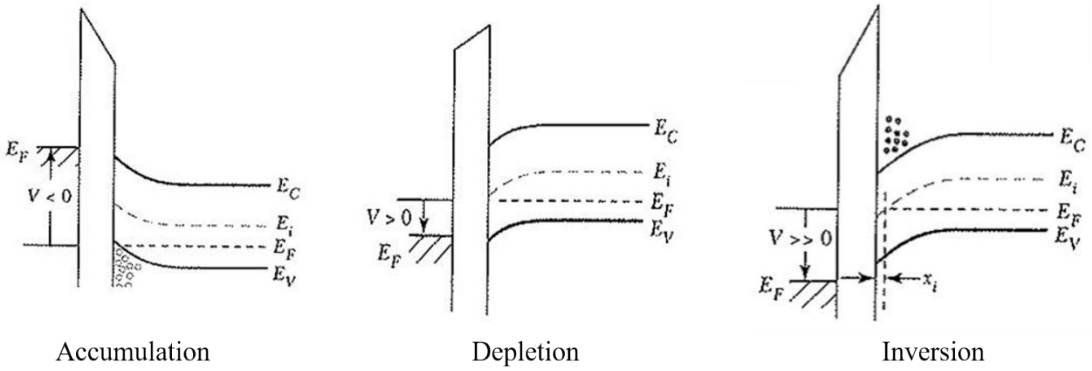


Figure S9-A | Accumulation, depletion, and inversion diagrams of MIS structure with p-type semiconductor [4].

The flat band voltage is, by definition, the voltage that causes the bands to be flat and is represented by equation S1 where Φ_{metal} is the metal work function, Φ_{Semi} is the silicon Fermi level, Q_{int} is the interface charge per unit area, Q_{bulk} is the bulk charge per unit volume, t_{ox} is the thickness of the oxide layer, and C_{ox} is the capacitance of that layer:

$$V_{fb} = \Phi_{Metal} - \Phi_{Semi} - \frac{Q_{int}}{C_{ox}} - \frac{Q_{bulk}t_{ox}}{2C_{ox}} \qquad (S1)$$

Figure S9-A illustrates the three regimes of MIS device behavior probed in capacitance-voltage (CV) analysis with a p-type semiconductor and low work function metal such that the flat band voltage is equal to zero volts. By applying a gate voltage that is negative of the flat band voltage (in the ideal case of Figure S9-A, less than zero), the metal (or gate) energy moves to more negative energy, which is up in this diagram since we draw band diagrams in terms of electron energy. Correspondingly, the Fermi level in the semiconductor moves down approaching half of the band gap $E_g/2$, and eventually exceeding it. This range of voltage is referred to as *accumulation* since the gate bias is opposite that of the majority carrier, causing those carriers (holes in the p-type semiconductor case at negative bias) to become accumulated in the semiconductor against the insulator as they are attracted toward the gate. Figure S9-A depicts this scenario on the far left showing an accumulation of holes in the valence band up against the insulator. Assuming the insulator is thick enough and defect-free such that the leakage current is low, this accumulation is successful and can be measured as a capacitance. Applying bias in the opposite direction of the flat band voltage (here positive of zero), causes holes to migrate away from the interface resulting in *depletion*. Eventually all of the holes become depleted as the Fermi level reaches the intrinsic point indicating that the hole and electron concentration is equal. As the gate bias is pushed further in this direction (here more positive) the Fermi level passes the intrinsic level until it eventually achieves an energy opposite its original position at flat band with respect to the intrinsic Fermi level. This voltage is referred to as the threshold voltage as it defines the transition from *depletion* to *inversion* where a minority charge layer begins accumulating. At the threshold voltage, the accumulated minority carrier density equals the density of acceptor or donor states given the semiconductor doping (in this case, electron density equals N_A). Therefore, the inversion layer charge is zero below this point and becomes linearly greater above this point.

Given an understanding of these three behavior regimes, the capacitance-voltage behavior of each can also be understood. The capacitance behavior is measured by stepping a DC bias over the MIS structure resulting in the different regimes of Figure S9-A and superimposing a smaller AC bias on top to measure the complex impedance at each gate bias at different AC measurement frequencies. Figure S9-B shows a typical CV profile, also for a p-type semiconductor. The flat band voltage is usually considered graphically to be the inflection point of the curve as shown here. More negative of the flat band voltage is the accumulation regime. Here the capacitance, charge stored, reaches the maximum value of C_{ox} and saturates. More positive of the flat band, the holes are depleted resulting in decreased capacitance down

to the minimum of the threshold voltage. If the AC frequency is low, on the order of several hertz to tens of hertz, the minority carrier generation is able to follow the AC signal and then the DC inversion regime is mapped by the AC probe. The capacitance rises again and saturates, ideally at the same value as the accumulation capacitance, given by equation S2 for a single insulator layer where C_i is the insulator capacitance (also commonly called C_{ox} in the field of metal-oxide-semiconductors (MOS) and in equation S1 earlier), ε_i is the dielectric constant of the insulator, ε_0 is the vacuum permittivity, and A is the area of the capacitor plate, in this work, the metal catalyst area:

$$C_i = \frac{\varepsilon_i \varepsilon_0 A}{t_i} \tag{S2}$$

When measuring at high frequency, hundreds of kilohertz to megahertz, the minority carrier generation cannot follow the AC signal, and no inversion capacitance is observed as shown in Figure S9-B by the red line denoted by HF for high frequency.

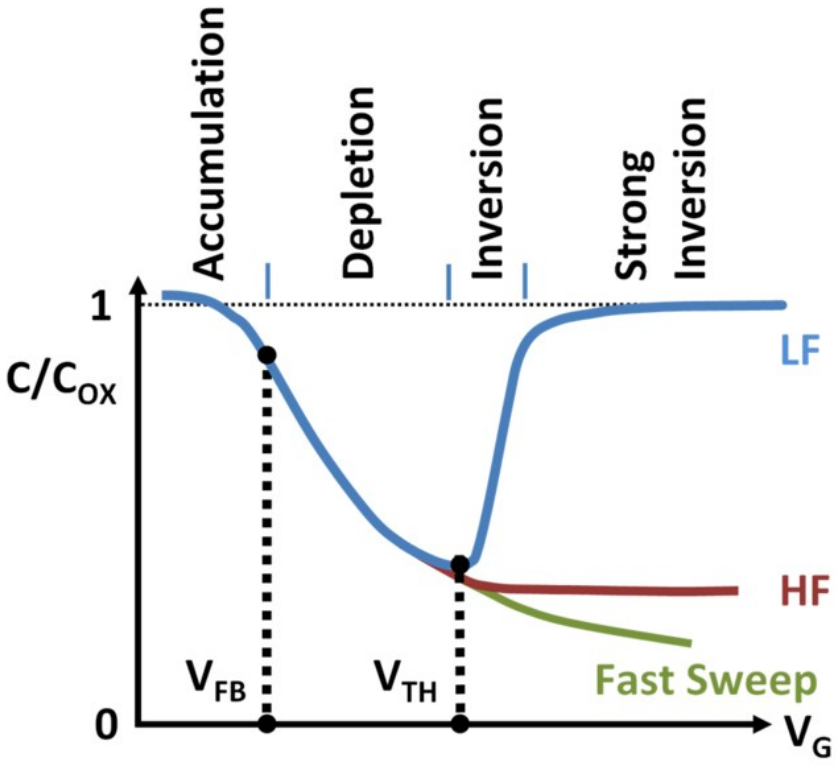
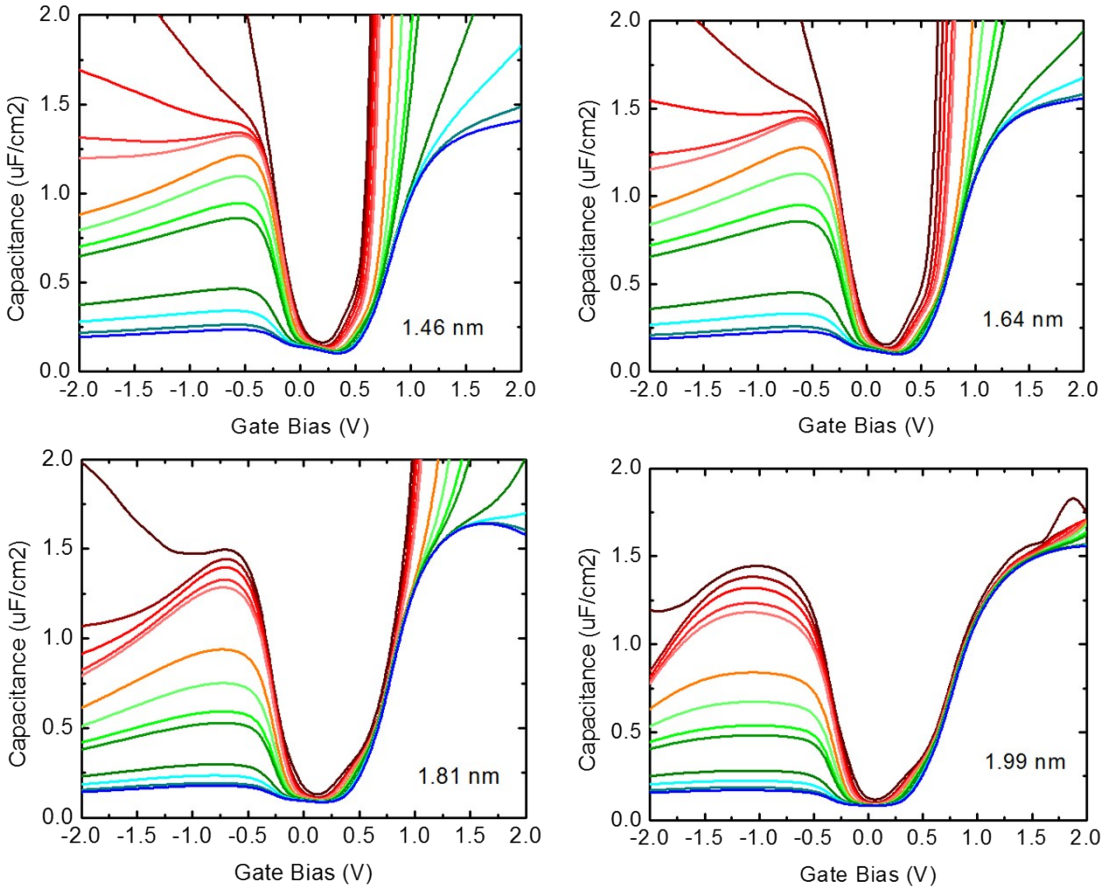


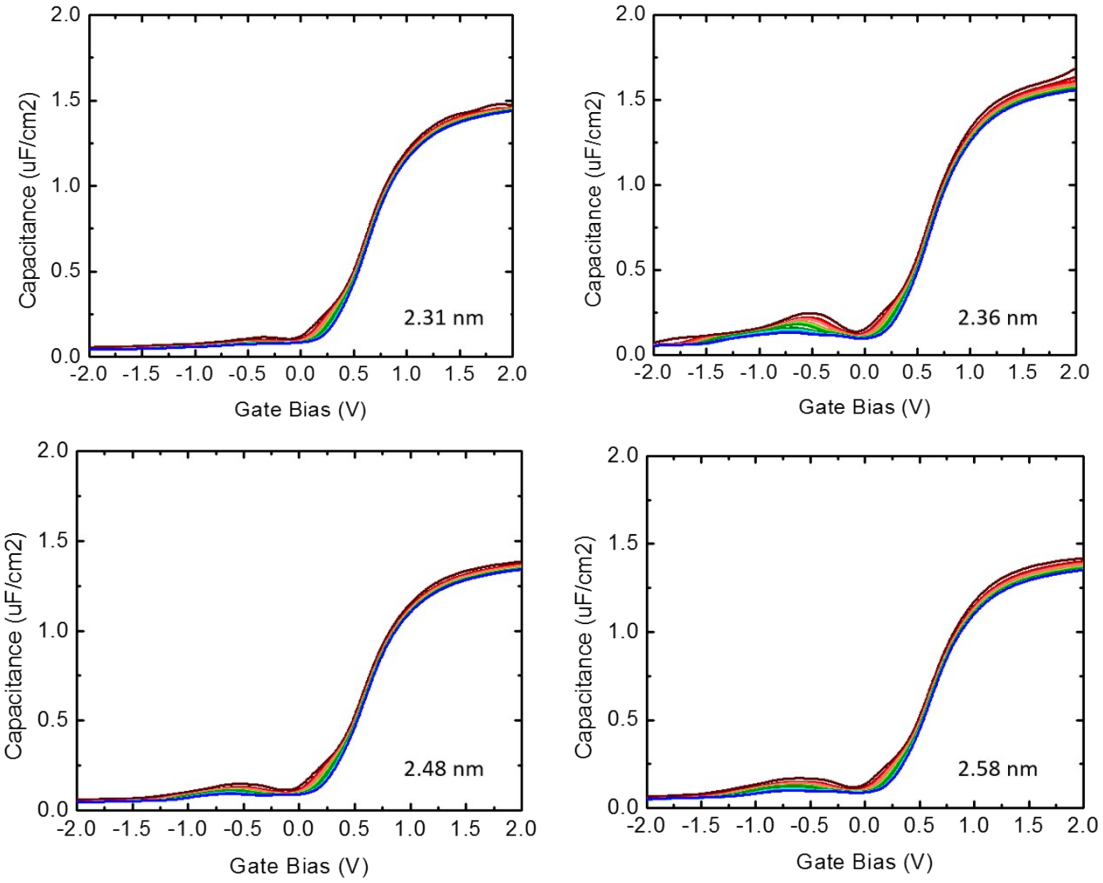
Figure S9-B | Ideal capacitance-voltage profile for p-type semiconductor showing the low frequency (LF) and high frequency (HF) curve.

Capacitance-voltage (CV) analysis of an n-type semiconductor is exactly the opposite of the behavior described here with accumulation being due to electrons in the conduction band,

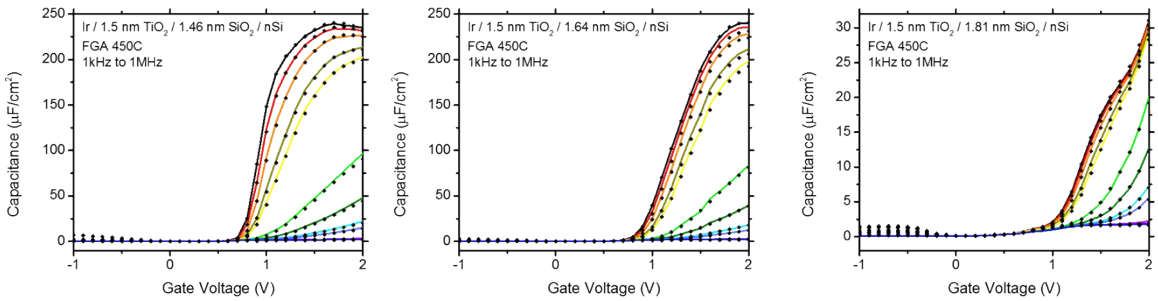
inversion resulting from holes in the valence band, and the capacitance profile of Figure S9-B flipped where accumulation occurs at more positive gate bias and inversion at more negative gate bias of the flat band voltage. Sections S10-S12 below as well as Figure 6 and 7 in the main paper show non-ideal capacitance voltage behavior of n-type silicon devices. The high leakage contributes to the curves shooting upward in accumulation particularly for low frequency scans (green to red color). This makes the flat band voltage hard to measure, except for the highest frequency curve as well as the oxide capacitance. Inversion behavior is also observed even at 1 MHz, which is non-ideal since minority carrier generation cannot follow an AC bias that rapid. This indicates a peripheral inversion effect as described previously [5]. All of these non-idealities are important for the understanding of MIS photoelectrochemical cell behavior. Juxtaposing them against ideal behavior and then simulating the non-ideality are the tools used in this work to help elucidate the physics at work and better extract important interface parameters.



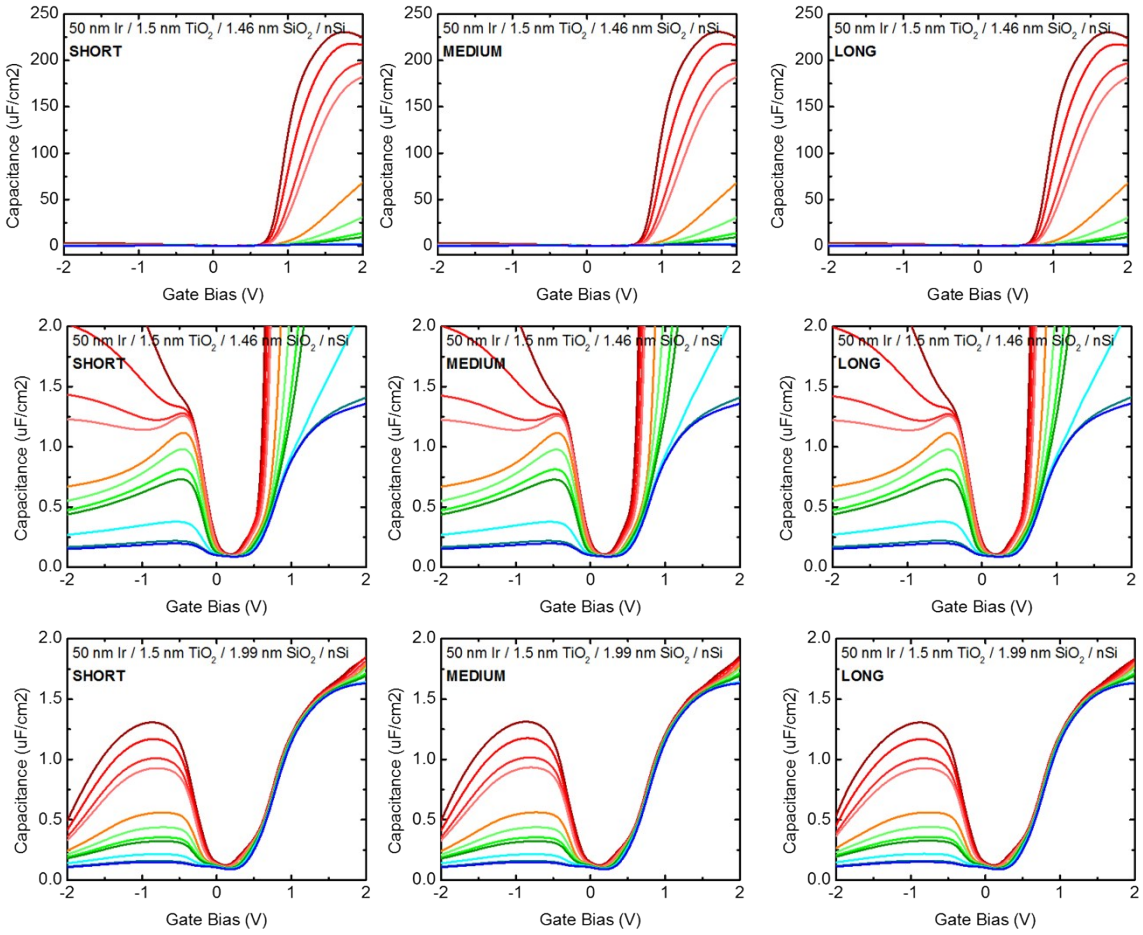
S10 | Capacitance voltage analysis with changing SiO_2 thickness. Capacitance-voltage curves for the first four SiO_2 thickness in the Ir / 1.5 nm TiO_2 / 'x' nm SiO_2 / nSi series. All are measured between 1kHz (dark red) to 1MHz (blue) with a 50mV AC probe bias at room temperature. The SiO_2 thicknesses are 1.46 nm, 1.64 nm, 1.81 nm, and 1.99 nm as measured by ellipsometry and written on the figures. A constant thickness of 1.5 nm of ALD-TiO_2 is deposited on top of each Si/SiO_2 substrate before deposition of a 50 nm thick iridium top gate for capacitance voltage analysis. The extent of the leakage non-ideality scales between the lowest SiO_2 thickness and higher SiO_2 thickness accordingly.



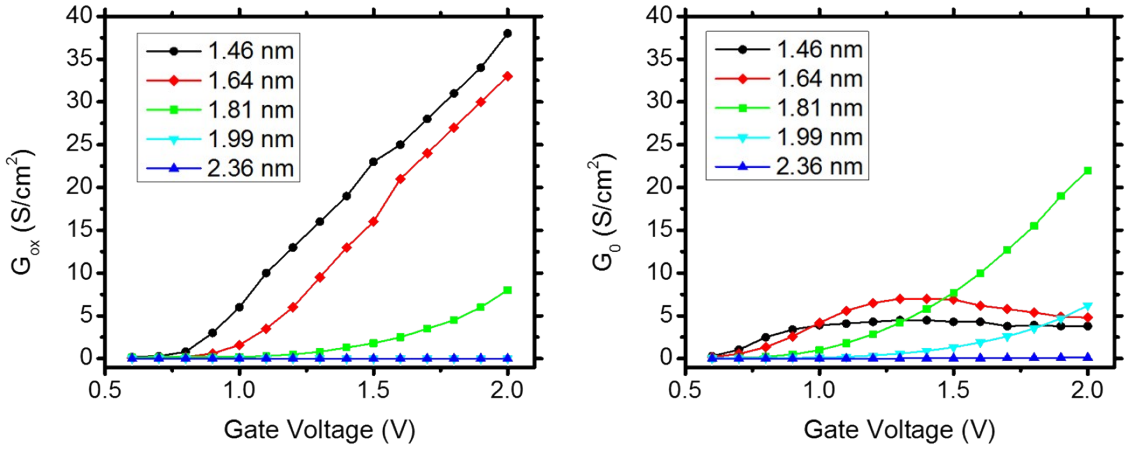
S11 | Capacitance voltage analysis with changing SiO_2 thickness. Capacitance-voltage curves for the last four SiO_2 thickness in the Ir / 1.5 nm TiO_2 / 'x' nm SiO_2 / nSi series. All are measured between 1kHz (dark red) to 1MHz (blue) with a 50mV AC probe bias at room temperature, identically to the first four anodes shown in S10.



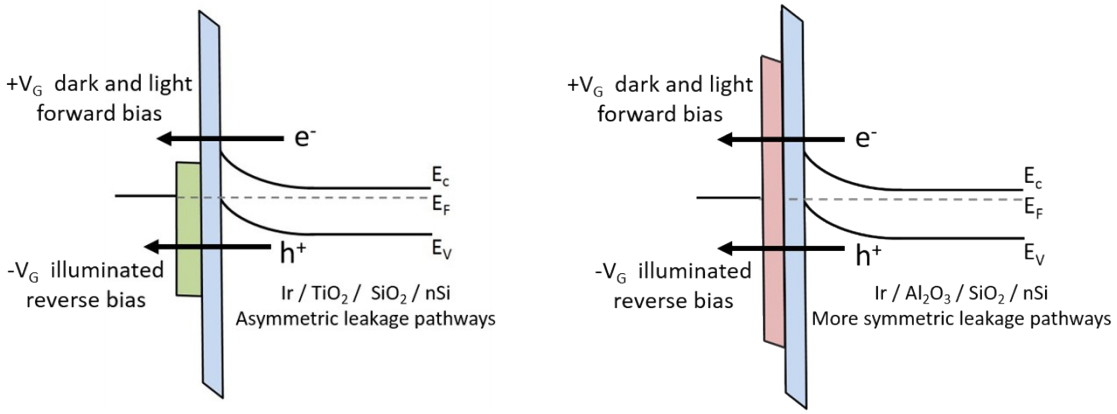
S12 | Non-ideal capacitance behavior of the thinnest three SiO_2 films fit with the model. Capacitance voltage curves for the empirical data (black circles) of subsequently thin SiO_2 layers compared with the simulated results (colored lines). The frequency dispersion goes from 1 kHz at the highest levels (black, red, orange) down to 1 MHz at the lowest measured capacitance (green, to blue, to purple). In each case, the fits are almost perfect showing that a simple circuit model containing capacitors for the semiconductor and oxide and, crucially, a leakage conductance G_{ox} around the oxide can adequately represent the data. The third frame shows the result for a SiO_2 layer thickness of 1.81 nm. Devices with thicker SiO_2 than this show very little non-ideal behavior as shown in S10 and S11 above.



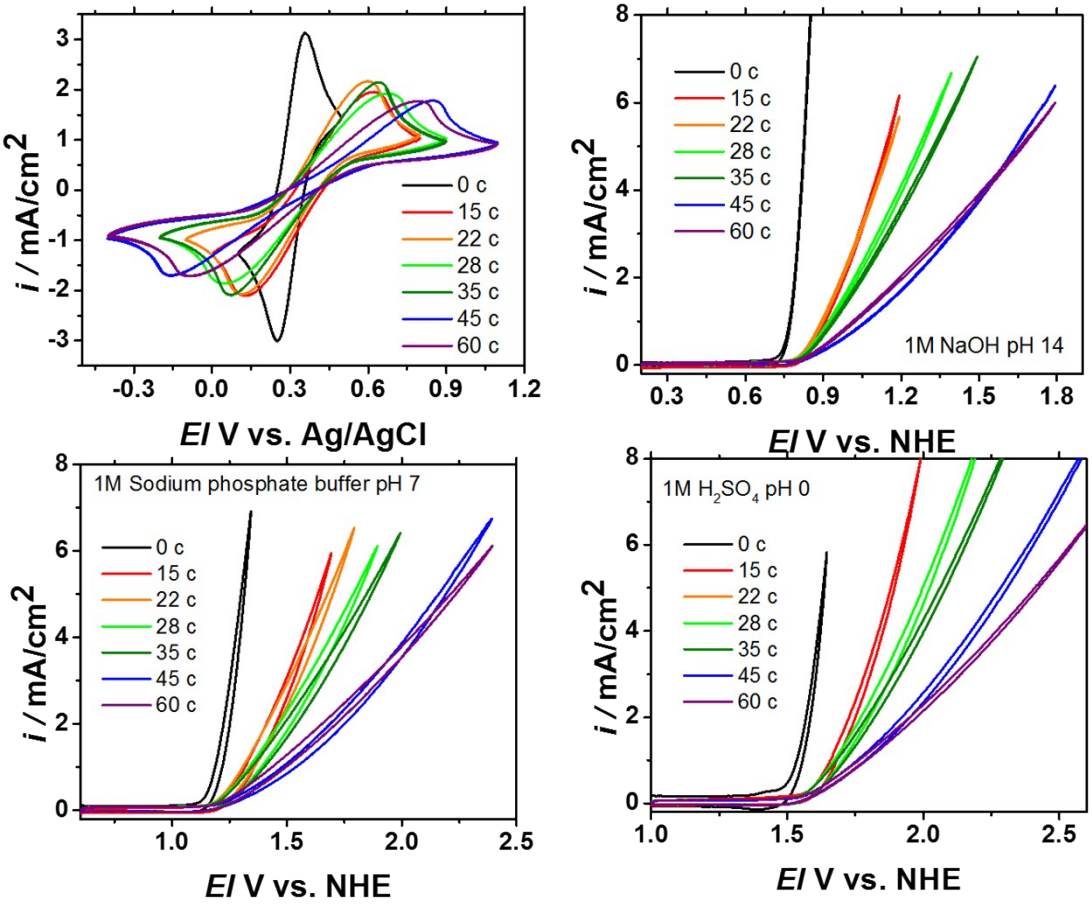
S13 | Non-ideal capacitance behavior measured at different integration time and DC scan rate. Capacitance voltage curves for the leakiest 1.46 nm SiO_2 interlayer (top row zoomed out to semiconductor capacitance, medium row zoomed into oxide capacitance) and the more capacitive 1.99 nm SiO_2 interlayer (bottom row) were measured at the three different integration time settings possible on the HP 4284A LCR meter. The short, medium, and long integration times shown above correspond to integrations of 30 ms, 65 ms, and 200 ms respectively. Given an averaging rate of 4, no delay, and step size of 0.1 V, these settings correspond to DC sweep rates of ~650 mV/s, ~215 mV/s, and ~55 mV/s respectively. These sensitivity plots were performed to check if the non-ideal capacitance voltage behavior was sensitive to changes in sweep parameters. As can be seen, no change is seen both for very leaky and the more capacitive structure for all three time settings. Changes to CV from different integration time typically indicate trapping contributions to the capacitance and are usually expected only for much thicker oxides.



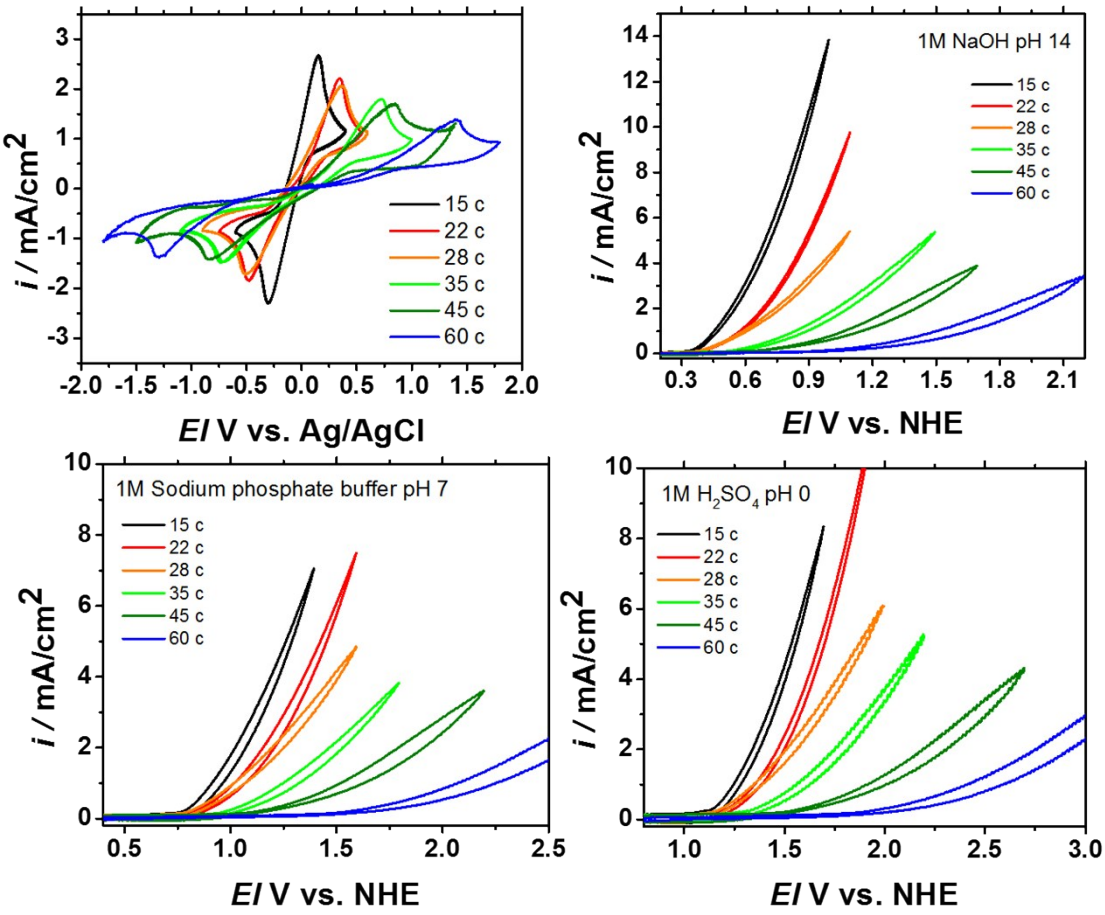
S14 | G_{ox} and G_0 fitting for capacitance model. The equivalent circuit model shown in Figure 7 (a) in the main paper is used to fit non-ideal capacitance voltage analysis for high leakage devices. Only a G_{ox} element, a leakage pathway through the oxides, is required to perfectly fit the capacitance voltage data, which is seen to move from a saturating C_{ox} value with thicker oxides to a higher saturation we ascribe to C_s. The left pane here shows the fitted G_{ox} value (S/cm^2) required to fit the data for each SiO_2 thickness as a function of voltage in the 50 nm Ir / 1.5 nm TiO_2 / 'x' nm SiO_2 / nSi device. As expected, the G_{ox} falls with thicker SiO_2 layers with a near exponential scaling with thickness. The tunneling relationship to barrier height or voltage is not as trivial, but scales similarly to the exponential to the square root of the barrier adjusted by pre-factors that decrease with increasing barrier height and make for a more linear curve. The G_{ox} behavior shown here agrees qualitatively with the tunneling modeling performed with Sentaurus and predicts overall device conductivities of the same order of magnitude for each SiO_2 thickness. In order to perfectly simulate both the imaginary (capacitance) and real (conductance) components of the complex impedance, one more element is needed. A shunt conductance, G_0 is required to fit the conductance data at low frequency as shown in the right pane here. For most thicknesses, this component is moderate to small and close to constant. Physically, G_0 corresponds to connections between the front and back contact that short the semiconductor capacitance as well as the oxide capacitance. Two reasonable contributions to this are (1) side conduction either as a result of cleaving or conductive ALD layers that may deposit conformably about the side of the sample or (2) shunt pathways through the oxide that form an Ohmic contact to the silicon substrate as opposed to a Schottky contact. Metallic shunts or high defect regions that pin the Fermi level locally could contribute to such pathways. Regardless, this represents a very minor contribution to the total conductance and does not affect the capacitance significantly.



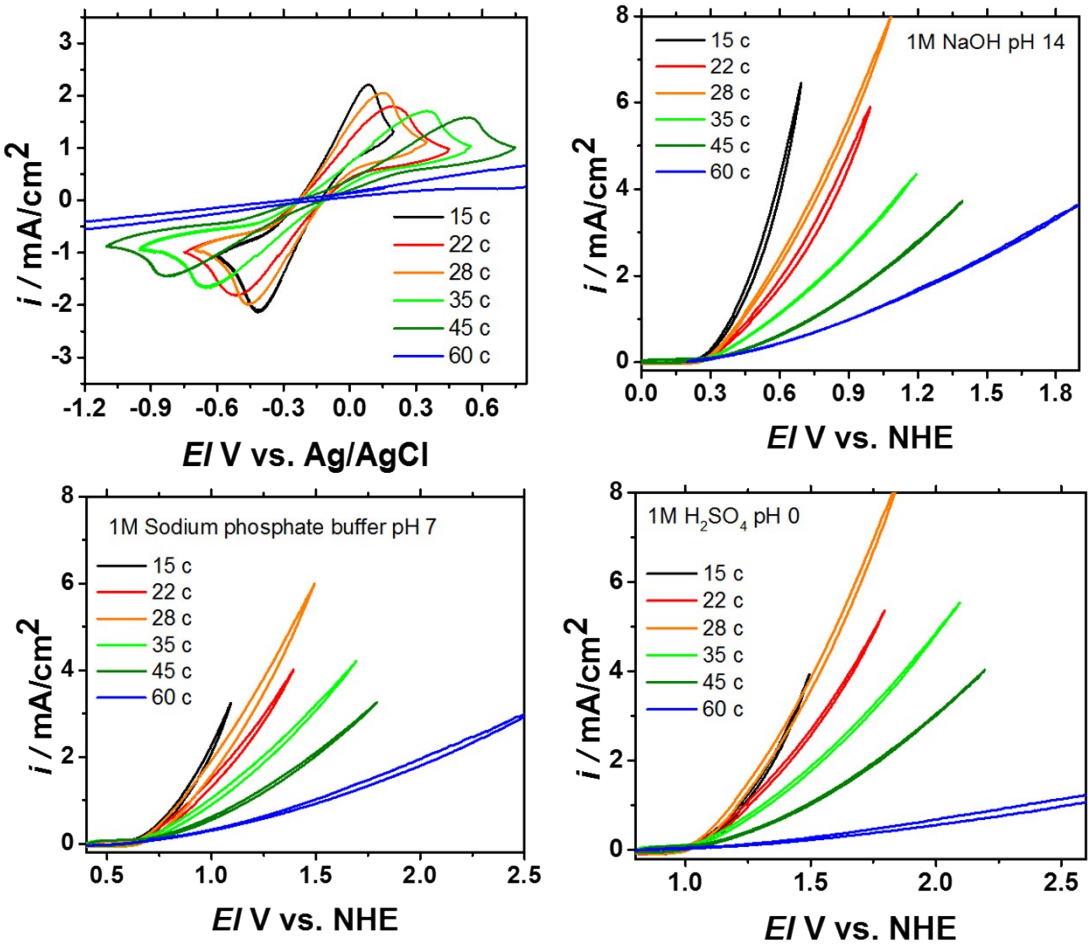
S15 | Si photoanode band diagrams showing difference in through-oxide leakage pathways between the TiO_2/SiO_2 and Al_2O_3/SiO_2 oxide systems. Under illumination and reverse bias, the through-oxide leakage pathway (as opposed to a thermionic or thermionic-field emission pathway) crosses the forbidden gap of both oxides. For ultrathin films, direct tunneling is possible [6] and hopping via trap states has been proposed in thicker films that exhibit high leakage [7-8]. The forward bias pathway is markedly different for the two systems, however. The conduction band offset (CBO) of TiO_2 to Si is on order -0.4V providing no additional barrier to electron leakage [9]. Thus only the SiO_2 provides significant resistance to electron leakage in the TiO_2/SiO_2 bilayer system. The conduction band and valence band offsets of Al_2O_3 to silicon are more symmetric, resulting in the forward bias through-oxide path also necessarily crossing both oxides' forbidden gap. Because of this, Al_2O_3/SiO_2 Schottky capacitors can have low leakage in both bias directions, whereas TiO_2/SiO_2 Schottky capacitors will only give a significant barrier to leakage in forward bias if the SiO_2 is significantly thick. Very large TiO_2 thicknesses will still add little DC resistance due to conduction via conduction band states. This asymmetry is independent of any considerations of forbidden gap leakage that may be due to trap-hopping as discussed in recent literature [7-8].



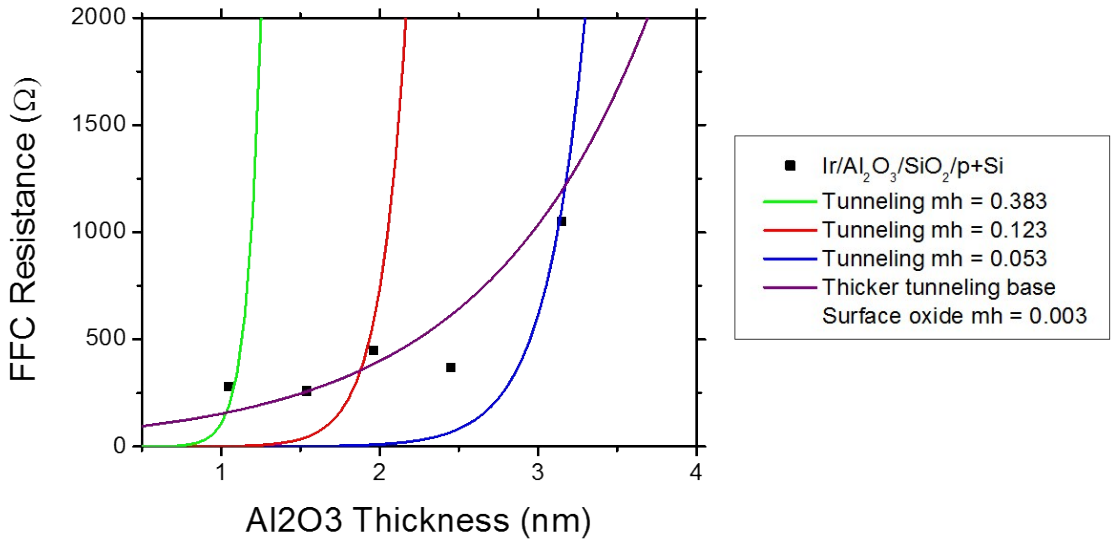
S16 | Electrochemistry data for Al_2O_3 protection of p^+Si. Electrochemical results taken in the dark for 2 nm Ir / 'x' cycles of ALD-Al_2O_3 / ~1.3 nm SiO_2 / p+Si. The growth rate was 0.72-0.75 Å/cycle.



S17 | Electrochemistry data for Al_2O_3 protection of nSi. Electrochemical results taken in the dark for 2 nm Ir / 'x' cycles of ALD-Al_2O_3 / ~1.3 nm SiO_2 / nSi. The growth rate was 0.72-0.75 Å/cycle.



S18 | Electrochemistry data for Al_2O_3 protection of p^+nSi. Electrochemical results taken in the dark for 2 nm Ir / 'x' cycles of ALD-Al_2O_3 / ~1.3 nm SiO_2 / p+nSi. The growth rate was 0.72-0.75 Å/cycle.



S19 | Total resistance of Al_2O_3/SiO_2 devices compared to tunneling predictions. FFC resistance data for Ir / 'x' nm Al_2O_3 / ~ 1.3 nm SiO_2 / p+Si anodes. Literature effective masses are all above 0.2 suggesting trends like the green line (—) which does not fit the data at all. Lowering the effective mass to around 0.1 (—) or 0.05 (—) shows that a direct tunneling model does not satisfactorily fit the data. The only way to obtain a decent fit given the slow increase in resistance and high baseline, is to assume a thicker tunneling base and an unrealistically low hole effective mass of 0.003 (—). A thicker tunneling base means that either the SiO_2 has grown more or the Al_2O_3 is considered non-homogenous with a bottom region over which tunneling occurs with a normal effective mass and then the leakier surface region. Neither model is expected to represent the true phenomenon. This indicates that these bilayer devices could not be satisfactorily modelled with a direct tunneling model alone. The deviance from tunneling is less severe than it is for the TiO_2 case showing that Al_2O_3 serves as an intermediate case as discussed in the main paper.

S20 | Sentaurus simulations parameters.

Material Property	Silicon	SiO_2	TiO_2	Al2O3
Bandgap (T = 300K), eV	1.12	9	3.2	6.1
Electron Affinity, ev	4.05	0.9	4.2	1.95
Dielectric Constant	11.7	3.9	32	8
Doping Density, cm^{-3}	1e21	N/A	1e17	N/A

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