Electronic Supplementary Material (ESI) for Lab on a Chip. This journal is © The Royal Society of Chemistry 2015

## Supplementary data:

1. Cross section of the optical housing



Figure 1: Cross section schematic of the handheld PCR system illustrating the optical path. Light emanating from the LEDs is filtered, then deflected by a dichroic mirror, and focused via lenses onto the VRC. A disposable glass slide separates the VRC from the micromachined silicon chip. The emitted fluorescence is collimated (using the same set of lenses), then passes through the dichroic mirror and a green filter prior to being captured by the photodiode.

## 2. Schematic of the PCR system



Figure 2: PCR electrical schematic showing four blocks of the fluorescent system inside the optical housing followed by transconductance operation amplifiers, by a generic amplifier and a Wheatstone bridge for temperature monitoring. The analog selector was used for further processing either the fluorescence or the temperature signals by the microcomputer (MCU) via an analog to digital converter (ADC). The processor also controls the dissipated Joule heat within the PCR chip and its temperature via a MOSFET driver.

## 3. List of components: Table 1

category	type	parameters	number
electrical	Square wave	Frequency: 1 kHz	6
	generator	duty cycle: 10 %	
	Power MOSFET	N-channel MOSFET	4
		with $R_{DS(on)}$ = 170 m $\Omega$	
	Power MOSFET	N-channel MOSFET	1
		with $R_{DS(on)}$ = 30 m $\Omega$	
	LED	Wavelength: 470 nm	4
		Luminous intensity:	
		7.2 – 12 cd	
		Diameter: 5 mm	
	photodiode	7.4 mm <sup>2</sup>	4
	Operation amplifier	diFET with bias	4
		current < 100 fA	
	Operation amplifier	Noise < 15 nV/vHz @	1
		1 kHz	
	Differential amplifier	Noise < 8 nV/vHz @	1
		1 kHz	
	Analog switch/analog	16 bit resolution, 2	1
	to digital converter	selectable	
		differential inputs	
	Analog multiplier	4-quadrant analog	1
		multiplier	
	Low pass filter	2 Hz cut off	1
	MCU	16 bit	1
		microprocessor	
	Graphic display	84 × 42 pixels	1
	Switched power	Generating DC	1
	supply	voltages: +5V, ±12V,	
		+18V	
thermomechanical	Micromachined	Custom layout,	1
	silicon chip	integrated with thin	
		film heater and RTD	
		sensor	
optical	Optical housing	Made by CNC	1
	Low pass filter	490 nm	2
	Dichroic mirror	495 nm	2
	Long pass filter	510 nm	1
	Lens	Diameter: 6.35 mm	4
		N.A.: 0.68	
		Focal length: 3.1 mm	

## 4. PCR chip layout



Figure 3 Layout of the PCR chip. The chip is square size with side of  $\approx$  15 mm. The distance between heater centers is  $\approx$  8mm.

- 5. PCR chip fabrication process
  - a. Starting substrate silicon wafers with diameter of  $\approx 100 \text{ mm}$
  - b. SiO<sub>2</sub> deposition by plasma enhanced chemical vapor deposition (PECVD) process with thickness of  $\approx 0.5~\mu m$
  - c. Au/Cr deposition by sputtering with thickness of  $\approx$  200 nm and  $\approx$  5 nm for Au and Cr, respectively
  - d. Contact lithography (Au/Cr patterning)
    - i. Positive photoresist (PR) spincoating with PR thickness between 1 and 2  $\mu m$
    - ii. PR pre-bake
    - iii. Soft contact exposure
    - iv. Postbake
    - v. PR developing
    - vi. Wafer spin drying
  - e. Au/Cr patterning by ion milling with secondary ion mass spectroscopy (SIMS) end point detection
  - f. PR removal by acetone and 2-n propyl alcohol or stripper
  - g. SiO<sub>2</sub> deposition by plasma enhanced chemical vapor deposition (PECVD) process with thickness of  $\approx$  0.5  $\mu m.$
  - h. Contact lithography (bond pads opening)
    - i. PR spincoating with PR thickness between 1  $\mu m$  and 2  $\mu m$
    - ii. PR pre-bake
    - iii. Soft contact exposure
    - iv. Postbake
    - v. PR developing
    - vi. Wafer spin drying
  - i. SiO<sub>2</sub> etching by  $\approx$  40 % NH<sub>4</sub>F and  $\approx$  49 % HF in ratio of  $\approx$  7 : 1 (BOE 7:1)
  - j. PR removal by acetone and 2-n propyl alcohol or stripper
  - k. Contact lithography (silicon etching)
    - i. PR spincoating with PR thickness between 8 and 12  $\mu m$
    - ii. PR pre-bake
    - iii. Soft contact exposure
    - iv. PR developing
    - v. Postbake
    - vi. Wafer spin drying
  - I. SiO<sub>2</sub> etching by BOE 7:1
  - m. Silicon etching by Bosch process through silicon water
  - n. PR removal by acetone and 2-n propyl alcohol or stripper
  - o. Chips drying by  $N_2$
  - p. Soldering chips to the printed circuit boards