Scaling of Sub-Micron Graphene Integrated Circuits

Electronic Supplementary Information

Massimiliano Bianchi,[a] Erica Guerriero,[a] Marco Fiocco,[a] Ruggero Alberti,[a] Laura Polloni,[a] Ashkan Behnam,[b] Enrique A. Carrion,[b] Eric Pop,[c] and Roman Sordan*[a]

Received Xth XXXXXXXXXX 20XX, Accepted Xth XXXXXXXXX 20XX
First published on the web Xth XXXXXXXXXX 200X
DOI: 10.1039/b000000x

Cutoff frequency. The most commonly used transistor performance metric is the cutoff frequency f_T; the intrinsic f_T can be very large in graphene FETs ($f_T \sim 400$ GHz)[1,2] due to large mobility in graphene, and compares favorably to that of conventional FETs.[3] The cutoff frequency was also found to scale as $f_T \propto L^{-1}$ similar to conventional semiconductor FETs.[1,3] However, the cutoff frequency is a measure of the internal transistor transit time rather than transistor functionality at high-frequencies. This is because the cutoff frequency is obtained from the small-signal current gain measured in a circuit in which the gate is driven by a current source while the output (between the source and drain) is shorted.[4] Use of an input current source makes the cutoff frequency independent of the gate resistance which is one of the main limiting factors affecting high-frequency response of FETs. Similarly, the short circuit between source and drain shorts the output conductance (in the absence of the parasitic source/drain series resistances) and therefore makes the cutoff frequency independent of the extent of the drain current saturation (shorted output also does not have any practical relevance).

Maximum frequency of oscillation. A more realistic figure of merit is the maximum frequency of oscillation f_{max} which represents the frequency at which the Mason's unilateral power gain[5] falls to unity. Since the power gain is obtained from a circuit in which the impedance of the input voltage source and the load impedance are finite,[4] both the gate resistance and output conductance influence the power gain and therefore f_{max}. For this reason graphene FETs exhibit much smaller f_{max} than other types of transistors, typically ~ 50 GHz.[6] By comparison, $f_{max} > 1$ THz has been obtained both in InP high electron mobility transistors[7] and heterojunction bipolar transistors.[8] In addition, f_{max} of graphene FETs was found to scale only weakly with the inverse gate length.[3] The maximum frequency of oscillation represents an important benchmark because it is an invariant quantity which allows comparison of different transistor technologies and accounts for real signal amplification.[5] However, it suffers from the requirements for device unilateralization and impedance matching which cannot be performed in realistic circuits.

Intrinsic gate delay. The typical figure of merit in a large-signal regime is the intrinsic gate delay CV/I which represents the time required to increase the voltage of the gate capacitor C_G by the large-signal output voltage swing ΔV when charged by a constant drain current I_D.[9]

References

1 Y. Wu, K. A. Jenkins, A. Valdes-Garcia, D. B. Farmer, Y. Zhu, A. A. Bol, C. Dimitrakopoulos, W. Zhu, F. Xia, P. Avouris and Y.-M. Lin, *Nano Lett.*, 2012, **12**, 3062–3067.
2 R. Cheng, J. Bai, L. Liao, H. Zhou, Y. Chen, L. Liu, Y.-C. Lin, S. Jiang, Y. Huang and X. Duan, *Proc. Natl. Acad. Sci. USA*, 2012, **109**, 11588–11592.
3 F. Schwierz, *Proc. IEEE*, 2013, **101**, 1567–1584.
4 F. Schwierz, H. Wong and J. J. Liou, *Nanometer CMOS*, Pan Stanford Publishing, Singapore, 2010.
5 S. Mason, *T. IRE Prof. Group Circ. Theory*, 1954, **CT-1**, 20–25.
6 Z. Guo, R. Dong, P. S. Chakraborty, N. Lourenco, J. Palmer, Y. Hu, M. Ruan, J. Hankinson, J. Kunc, J. D. Cressler, C. Berger and W. A. de Heer, *Nano Lett.*, 2013, **13**, 942–947.
7 R. Lai, X. Mei, W. Deal, W. Yoshida, Y. M. Kim, P. H. Liu, J. Lee, J. Uyeda, V. Radisic, M. Lange, T. Gaier, L. Samoska and A. Fung, Int. El. Devices Meet., 2007, pp. 609–611.
8 J. Hacker, M. Urteaga, M. Seo, A. Skalare and R. Lin, Proc. IEEE MTT-S Int. Microwave Symp., 2013, pp. 1–3.
9 R. Chau, S. Datta, M. Doczy, B. Doyle, B. Jin, J. Kavalieros, A. Majumdar, M. Metz and M. Radosavljevic, *IEEE T. Nanotechnol.*, 2005, **4**, 153–158.

[a] *L-NESS, Department of Physics, Politecnico di Milano, Polo di Como, Via Anzani 42, 22100 Como, Italy. E-mail: roman.sordan@polimi.it*
[b] *Electrical & Computer Engineering, University Illinois Urbana-Champaign, Urbana IL 61801, USA.*
[c] *Electrical Engineering, Stanford University, Stanford, CA 94305, USA.*