Electronic Supplementary Material (ESI) for Nanoscale.

Supporting Information

Ultralow-power Non-volatile Memory Cells based on P(VDF-TrFE) Ferroelectric-gate CMOS Silicon Nanowire Channel Field-Effect Transistors

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1. Four probe measurements

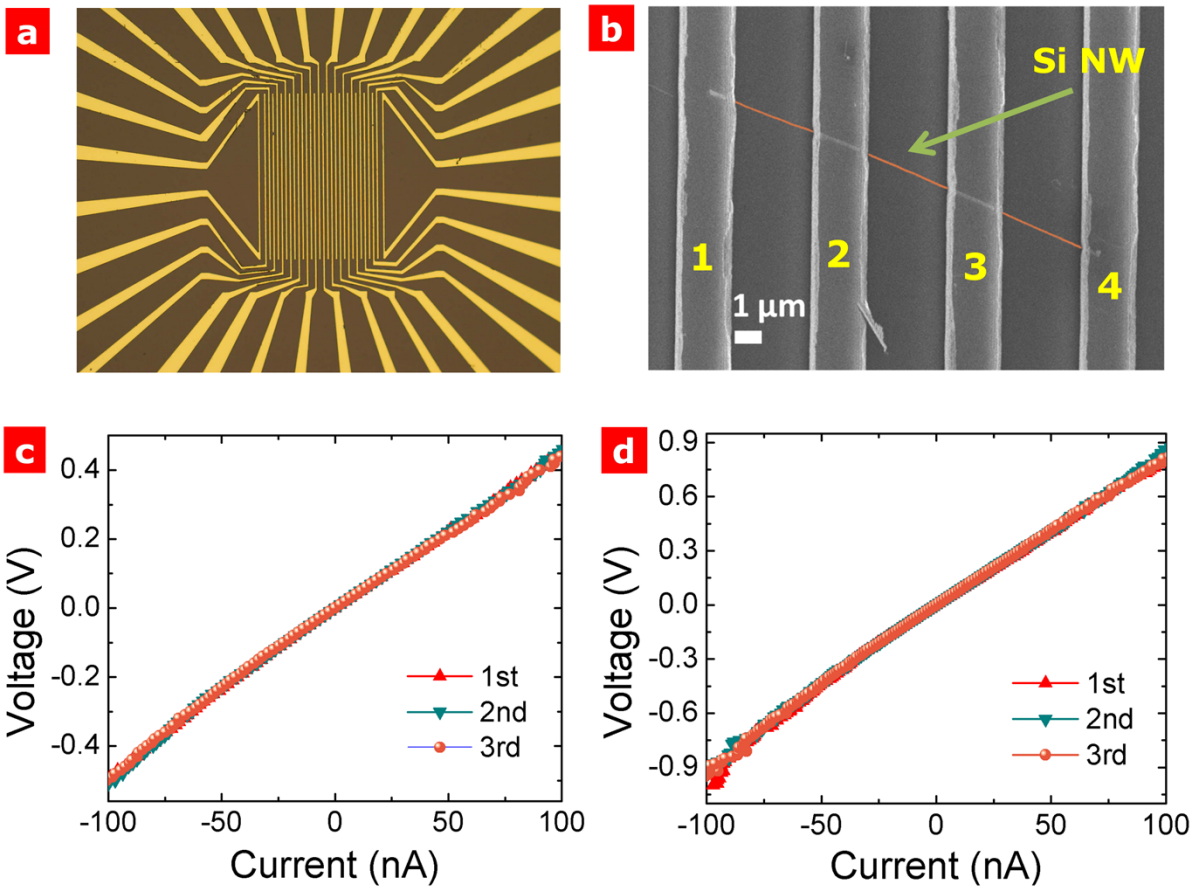

Fig. S1 (a) Optical and (b) FE-SEM images of Si NW FET devices; four probe measurements of n-type (c) and p-type (d) Si NWs.

The n-type Si NW resistance (R) of 4.44×10^6 Ω was extrapolated from the linear region of the current–voltage curve of four-probe measurements from Fig. S1c. The resistivity $\rho = 0.21$ Ω cm was calculated according to $\rho = RA/L$, where $A = \pi r^2$ is the Si NW cross section, L is the conducting channel length of the nanowire (~5 µm), and r is the radius of the nanowire (~27.5 nm). The resistance, $R = 8.1 \times 10^6$ Ω, and resistivity, $\rho = 0.38$ Ω cm, were calculated for p-type Si NWs from Fig. S1d.

2. Electrical transport properties of single n- and p-type Si NW FET devices

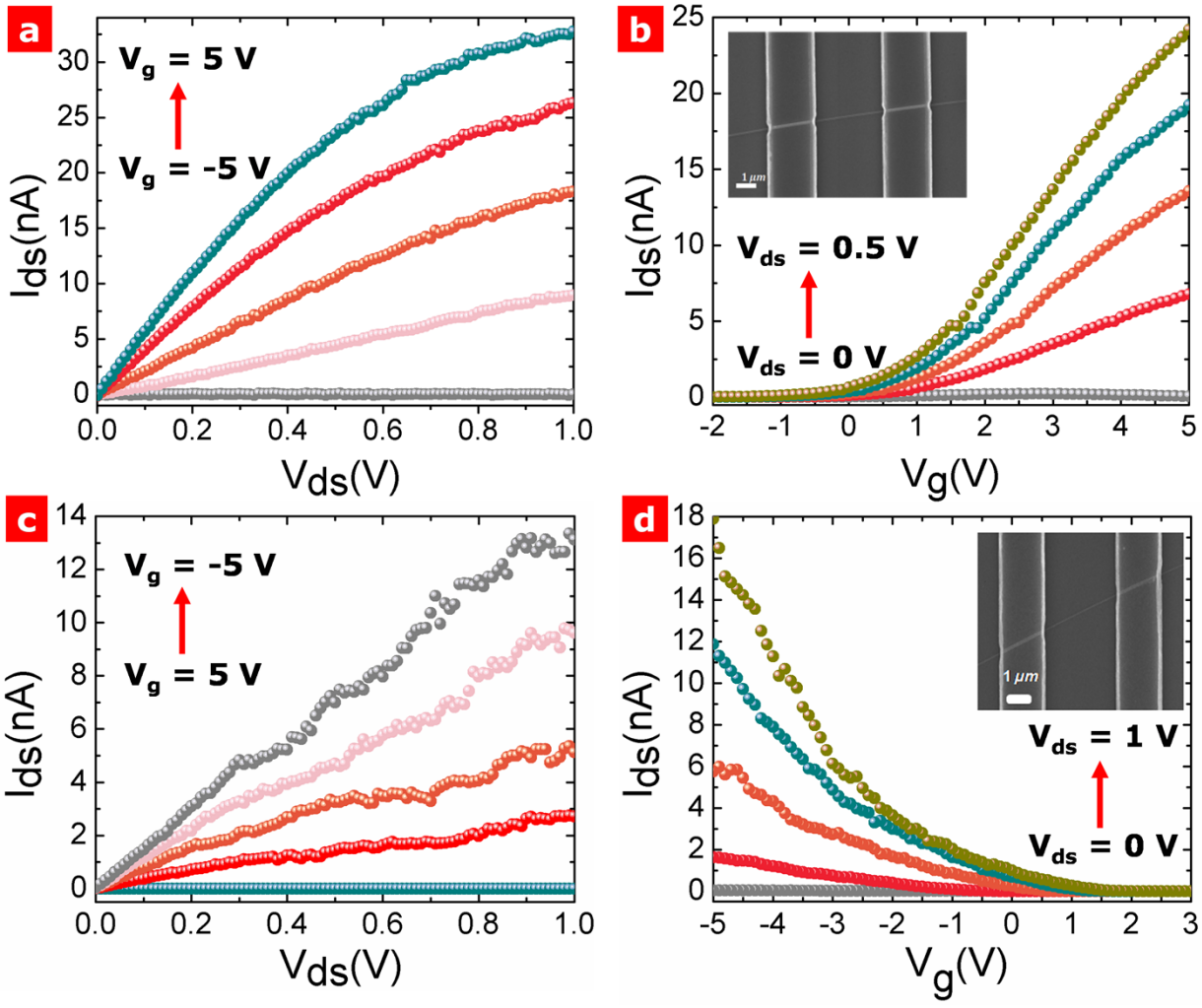

Fig. S2 Electrical transport properties of single n- and p-type Si NW FET devices at ambient conditions. (a), (c) I_{ds}–V_{ds} output characteristics and (b), (d) I_{ds}–V_g transfer characteristics of n- and p-type Si NW FETs, respectively.

To investigate the electrical properties of n-type and p-type Si NWs, we prepared typical NW FETs on a 100 nm thick SiO_2 layer on a heavily boron doped Si (p++ Si) substrate; the a-Si acted as a back gate electrode. Figure S2a shows the drain current versus drain-source voltage (I_{ds}–V_{ds}) curves for a single n-type Si NW FET. The conductance of the NW increases monotonically as the gate potential increases from −5 V to +5 V, exhibiting a typical n-type Si NW FET behavior.

Figure S2b shows the drain current versus gate-source voltage (I_{ds}-V_g) curves obtained by sweeping the gate voltage continuously from −5 V to 5 V at a drain voltage ranging from 0 to 0.5 V. The transconductance (g_m) and field effect electron mobility (μ_e) of the back gate NW FETs were determined from the I_{ds}–V_g curves using the following equations: $g_m = dI_{ds}/dV_g$ and $\mu_e = g_m L^2/C_{ox}V_{ds}$.[1] The gate oxide capacitance (C_{ox}) of a cylindrical wire on a planar substrate can be estimated by $C_{ox} = 2\pi\varepsilon_r\varepsilon_0 L/cosh^{-1}(1+ t_{ox}/r)$ using a relative dielectric constant (ε_r) of 3.9, a SiO_2 gate dielectric layer thickness (t_{ox}) of 100 nm, a nanowire conducting channel length (L) of approximately 5 μm, and a nanowire radius (r) of approximately 27.5 nm. For n-type Si NW FETs on a SiO_2/Si substrate, a threshold voltage (V_{th}) of −1 V and a transconductance (g_m) of 9.7 nS were extrapolated from the linear region of the I_{ds}–V_g curve at a value of 0.5 V for the V_{ds}. The field-effect electron mobility (μ_e) and resistivity (ρ) for Si NW was calculated from four-probe measurements and found to be 9.9 $cm^2\ V^{-1}\ s^{-1}$ and 0.21 Ω cm, respectively (Fig. S1c). Electron carrier concentration (n_e) was calculated to be 2.58×10^{17} e/cm^3 using the equation, $n_e = C_{ox}V_{th}/e\pi r^2 L$.[2] The subthreshold swing given as $S.S = log[dV_g/d(logI_{ds})]$ was estimated to be 168 mV dec^{-1}.

The same calculation method is applicable for p-type Si NW FETs. A V_{th} of 1 V, g_m of 14.1 nS, and a field effect hole mobility (μ_h) of 7.2 $cm^2\ V^{-1}\ s^{-1}$ were calculated from Fig. S2c and d, and ρ was estimated to be 0.38 Ω cm from four-probe measurements (Fig. S1d in the Supporting Information). Hole carrier concentration (n_h) was estimated to be 2.58×10^{17} h cm^{-3} using the equation $n_h = C_{ox}V_{th}/q\pi r^2 L$.[2] The subthreshold swing ($S.S$) value was approximately 216 mV dec^{-1}. The subthreshold swing values of n-type and p-type Si NW FETs are small enough for low power consumption devices.

References

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