SUPPLEMENTARY INFORMATION

Lateral graphene p-n junctions formed by graphene/MoS₂ hybrid interface

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Figure S1. Fabrication process of the devices. (a) Monolayer MoS₂ grown by CVD method on Si/SiO₂ substrate. (b) Graphene/PMMA microstamp is transferred on MoS₂ by a site-specific transfer-printing method. Part of the graphene is on the MoS₂ and the other graphene portion is on the SiO₂ substrate. (c) To obtain appropriate structure for device fabrication, the PMMA is patterned by electron beam lithography (EBL) technique. (d) Excressent parts of MoS₂ and graphene are removed by Plasma Etching technique. (e) PMMA layer is dissolved in acetone. (f) Deposition of Pd/Au electrodes by EBL, metal deposition, and lift off procedures.



Figure S2. Figure S2. Transfer curves of the graphene/SiO₂ and graphene/MoS₂ field effect transistors. The back gate voltage was swept from -60 to 60 V, then back to -60 V immediately. The gate voltage sweeping rate is 0.5V/s at V_{ds} =50 mV. A clear hysteresis behavior is observed in graphene/SiO₂ region. Nevertheless, the graphene on MoS₂ does not show the similar hysteresis behavior. Compared to SiO₂ substrate, monolayer MoS₂ has better crystal structure with very few carrier trapping centers and gas molecular adsorption sites, which restrains the hysteresis behavior.



Figure S3. Zoom in the time scale of the photoresponse in Figures 3c and 3d to clearly show the rise and fall processes of the V_{OC} and I_{sc} .



Figure S4. (a) Transfer curves of graphene/MoS₂ vertical region (electrodes D-C) with and without laser illumination near the graphene/electrode interface. (b) Photocurrent $[I_{ph} = I_{ds}(\text{laser on}) - I_{ds}(\text{dark})]$ obtained from the data in Figure S3a. The zero photocurrent point is introduced by metal-graphene interface as reported before. (c) Transfer curves of graphene/SiO₂ region (electrodes A-B) with and without illumination.



Figure S5. (a) Seebeck coefficients of the graphene on SiO_2 and MoS_2 as sweeping gate voltage. (b) Evolution of the difference of the Seebeck coefficients under gate voltage modulation.