Supplementary Information:

Transfer Printing of CVD Graphene FETs on Patterned Substrates

T. S. Abhilash[1], R. De Alba[1], N. Zhelev[1], H. G. Craighead[2]and J. M. Parpia[1]

[1]Department of Physics, Cornell University, Ithaca, NY 14853, USA.
[2]School of Applied and Engineering Physics, Cornell University, Ithaca, NY 14853, USA.
E-mail: jmp9@cornell.edu

1) Graphene FET device structure:

The graphene channel field effect transistor device structure and the circuit diagram used for measurement of source-drain current as a function of back-gate bias is shown in Fig.S1. Here graphene is transferred on to pre-patterned source-drain electrodes.

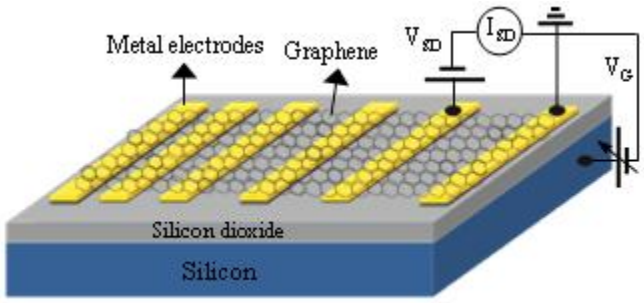

Fig.S1: Illustration of graphene device structure and the circuit diagram corresponding to measurement of I_{SD} (V_G).

2) Scanning Electron Microscopy Image:

High magnification SEM image of a selected area of graphene transferred to Si/SiO_2 substrate is shown in Fig. S2.

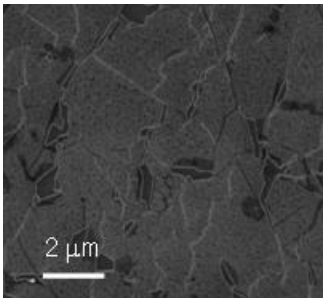

Fig.S2: SEM image of graphene transferred to Si/SiO_2 substrate.

3) SEM and AFM Analysis:

Fig.S3 shows SEM and AFM amplitude error images (10 μm x 10 μm) acquired at boundary between graphene on Ti/Au metal contact and Si/SiO_2 substrate. AFM amplitude error image showed best sensitivity to the presence of graphene. AFM image confirmed the coverage of graphene over Si/SiO_2 substrate. SEM image shows the continuous coverage of graphene over substrate and metal contacts.

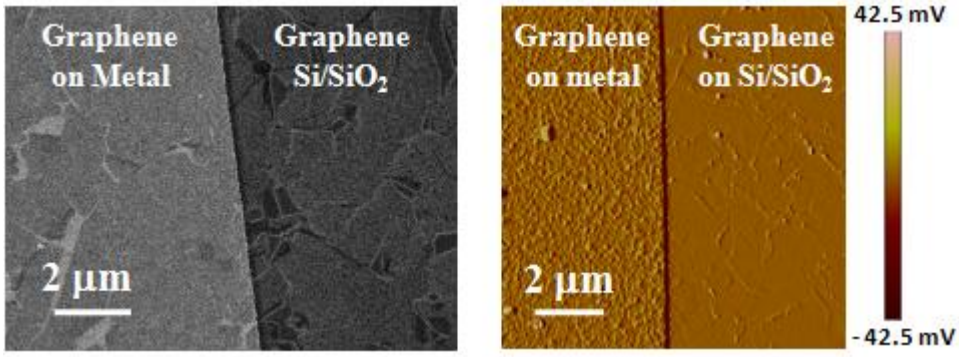

Fig.S3: SEM and AFM amplitude error images acquired at boundary between graphene on Ti/Au metal contact and Si/SiO_2 substrate.