Electronic Supplementary Material (ESI) for Nanoscale.
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Supplementary Information

Corrosion Resistant Three-Dimensional Nanotextured Silicon for Water Photo-Oxidation

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I. Experimental Methods

Material Fabrication. Stain etching of n+ (100) silicon was initiated in a fume hood on a stir plate by placing 3 cm X 3 cm wafer pieces in 10 mL of nano-pure water, adding 5 mL of HNO_3 and then 1 mL of 40% HF drop by drop. The entire solution was placed on a shake plate oscillating at 85 rpm. The reaction should run for 15 minutes form the initial formation of bubbles on the wafer surface. For carbon coating the material is then loaded into a chemical vapor deposition (CVD) furnace. The system should be evacuated, pressurized with argon and then heated to 650°C under 200 sccm of H_2 and 1 sLm of Ar, at 650°C 10 sccms of C_2H_4 are allowed to flow and the temperature is ramped to 750°C, at 750°C temperature is held constant for 10 minutes and then ramped to 850°C, at 850°C the temperature is held for 10 minutes and then C_2H_4 flow is stopped and the material is cooled under Ar and H_2 flow. Hydrogen terminated controls were prepared by soaking n-type silicon wafers in ethanol with a low concentration of

HF for 1 hour. The material is examined under Renishaw Raman with a 785nm laser. Scanning Electron Microscopy was carried out with Raith e-line and Transmission Electron Microscopy was carried out using Osiris FEI.

Electrochemical Testing. The material was probed with electrochemical testing using a Metrohm Autolab multichannel testing unit. Electrochemical impedance spectroscopy (EIS) measurements were made with 3-electrode setup, passivated silicon as anode, platinum as counter electrode, and an Ag/AgCl reference electrode in 0.1M Na_2SO_4. Measurements were made at solution potential of 0V with testing amplitude of 10mV over frequency ranges 20mHz to 10kHz. To probe the effectiveness of the material as a photoanode the material is tested with the same 3-electrode setup in 1M NaOH under illumination of 1 sun. Cyclic voltammetry of the system was acquired across the voltage range of -0.3V and 1.0V vs. Ag/AgCl at scan rate of 20mV/s.

II. EIS Discussion

Examining Figure 3A and Table 1 more closely it is clear that the fitting circuit employs a combination of constant phase elements and resistive elements. These are arranged such that there is a solution resistance across the cell, a resistive and capacitive element (constant phase element) probing the dielectric behavior of the coating and resistance in conjunction with this element from pores in the coating inhibiting the dielectric behavior, and finally a resistive and capacitive element probing the double layer of ions developed along the surface of the material as potential is developed and the resistance of the coating limiting this. In order to obtain low X^2 values from R-C circuit fits constant phase elements were employed to model imperfect capacitors. If the constant phase element is a perfect capacitor N=1. The appearance of an

imperfect capacitor in Nyquist plots (Fig S1) is a flatted semicircle. From Table 1 one can see that our passivated material had capacitive elements of either perfect or very close to perfect capacitors (0.95). This is true for most of the constant phase elements used in our models. The element with the farthest deviation from a true capacitor is the dielectric behavior of the textured material following stain etching. This is probably due to its high reactivity preventing its H-terminated sites from acting in a dielectric manner.

Looking closely at the other values reported it is observed that the solution resistance has little deviation across samples and the pore resistance is highest for the stain etched material and lowest for the passivated and textured material. The low pore resistance of the passivated material suggests very few pinholes in the coating. The high pore resistance of the stain etched material is a result of the H-termination not being a strong enough passivation in solution, since the H-termination of the textured material fails to act in a dielectric manner; pin holes are easily formed in the layer. The coating resistance of both the H-terminated flat wafer and stain etched wafer reveal similar values, since both materials are H passivated. The coating resistance of the carbon passivated and textured material is over 50Xs that of the others. The capacitance of the coating is lowest in the flat wafer and highest in the carbon passivated one. The coating capacitance of the stain etched material is about half that of the carbon passivated but somewhat high, this could be due to the reactive nature of the material, readily forming a native oxide species in the basic solution that are more dielectric in behavior compared to single a hydrogen atom. Finally the double layer capacitance of the carbon-passivated material is highest and is about 3 times that of the other two samples. This is due to the conductive nature of the coating. Since the graphenic coating is highly conductive it still facilitates the proper development of a surface double layer, losses of conductivity at the H-terminated samples will limit this.

The trends discussed from these models were consistent across many sampled materials of these conditions.

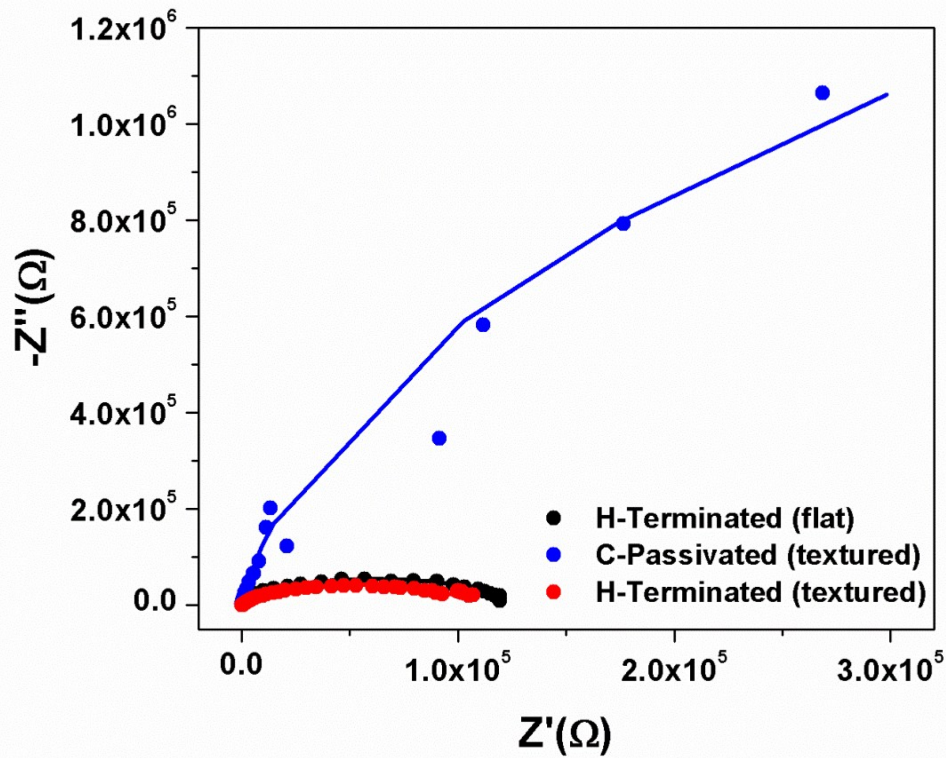

Fig S1- Nyquist plot for H-terminated flat wafer, textured and C-passivated textured wafer.

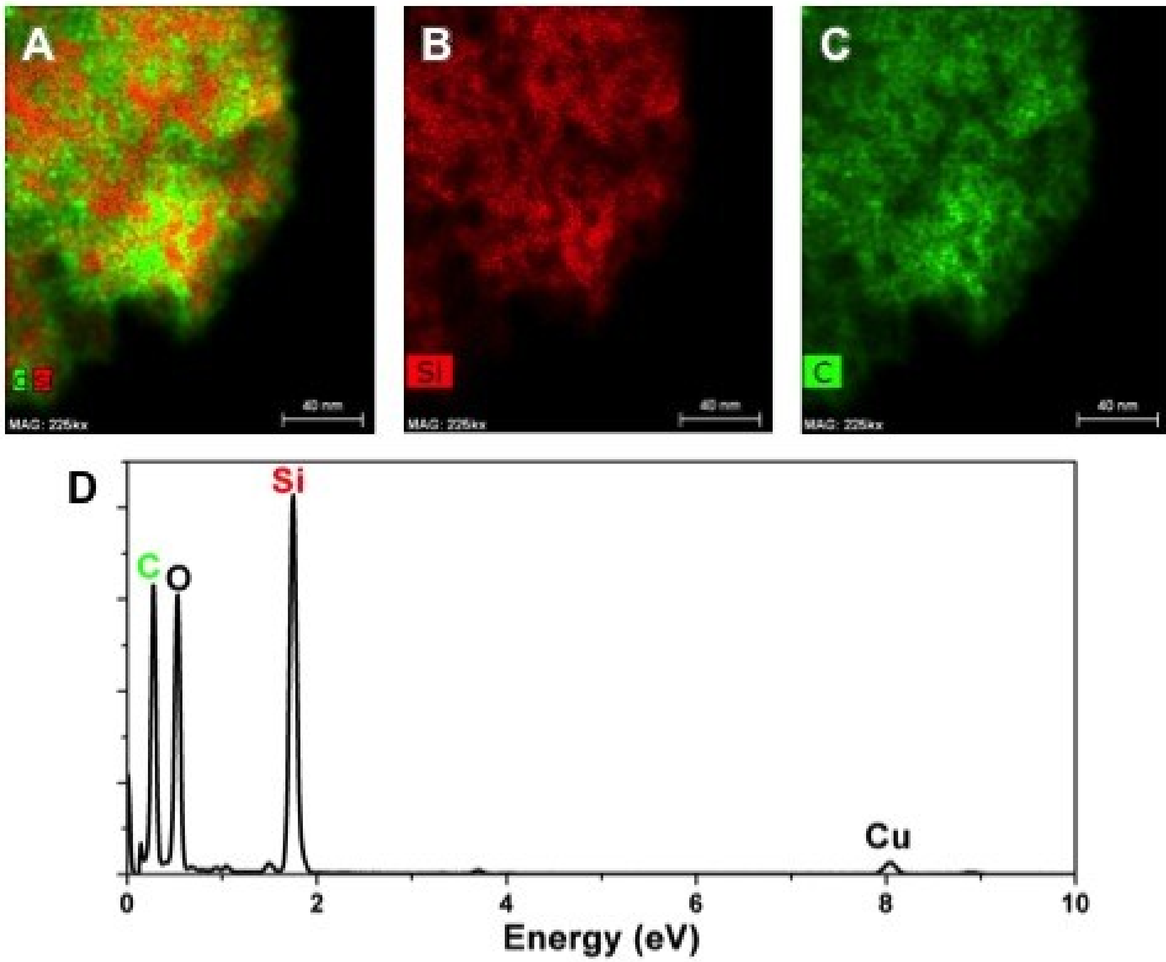

Fig S2- STEM EDS map of C-Passivated (textured) sample (A) showing carbon and silicon and (B) and (C) showing individual elements Si, and C respectively to reveal full passivation, (D) is the full x-ray energy spectra revealing dominant elements, C, O, Cu, and Si (where O and Cu are picked up from the TEM grid).

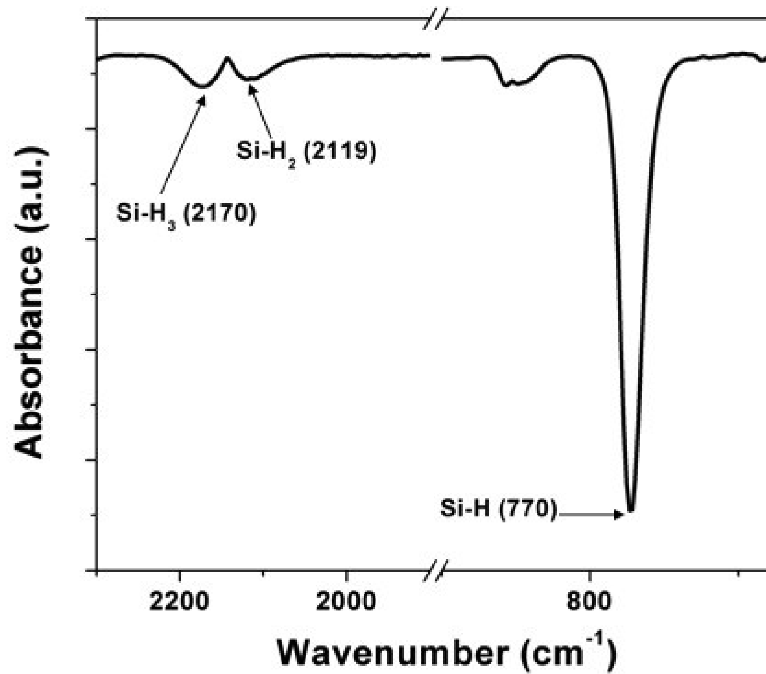

Fig S3- FTIR spectra of H-terminated n-type silicon with specific stretches corresponding to H-terminated Si sites labeled.

The FTIR spectra shows silicon stretch modes which agree well with reported values in literature.[1-5] The unlabeled peak around 850 cm^{-1} is likely silicon fluorine stretching as a result of removing the material from the etchant. [6]

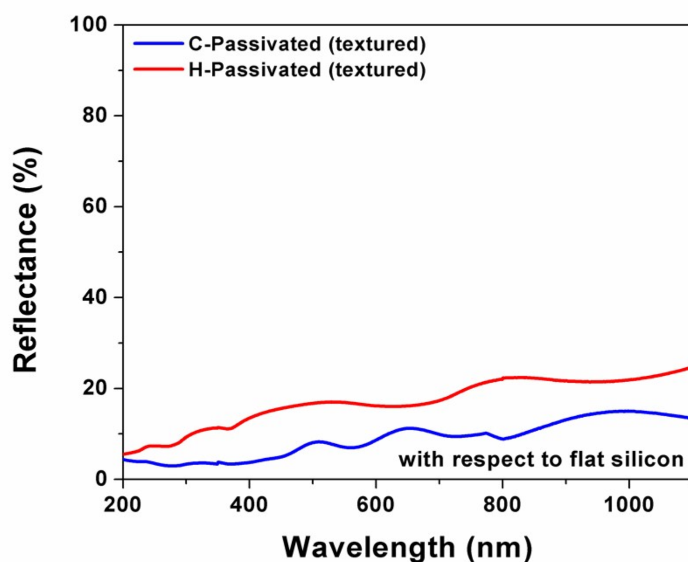

Fig S4- Wavelength dependent reflectance analysis of nanotextured silicon samples both with and without few-layered defective graphene passivation. In each case, the reflectance is plotted relative to a flat silicon reference. Overall, this generally indicates between 80-90% decrease in reflectance for nanotextured surfaces compared to flat silicon, confirming the light trapping effect of the textured surface.

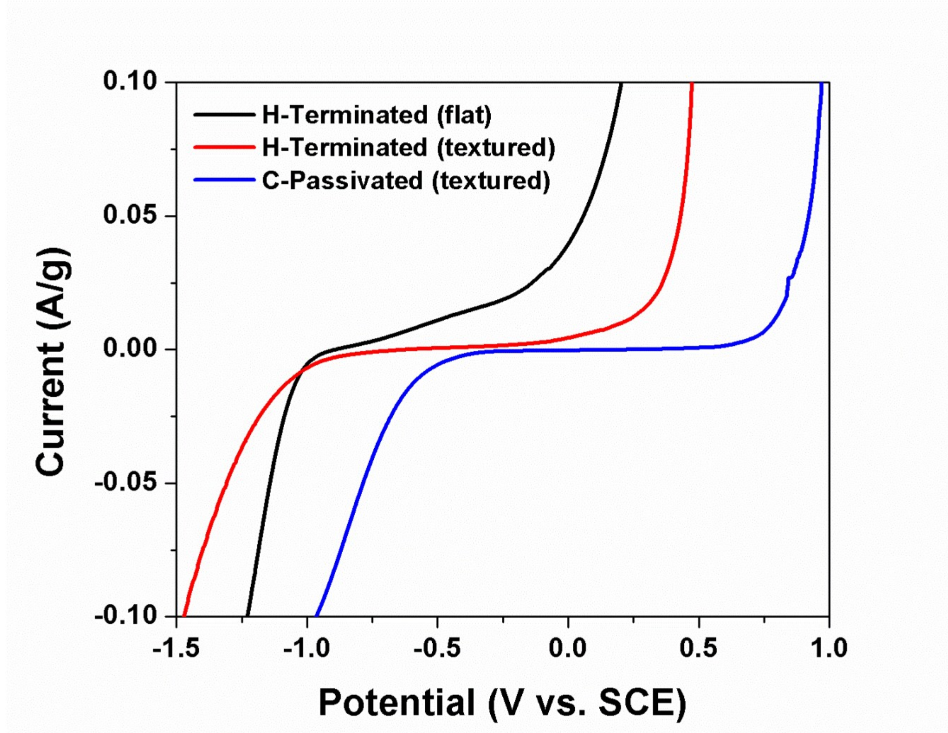

Fig S5- Linear Scanning Voltametry for H-terminated flat wafer, textured, and C-passivated textured wafer (log scale of this data corresponds to Tafel plot results plotted in main text)

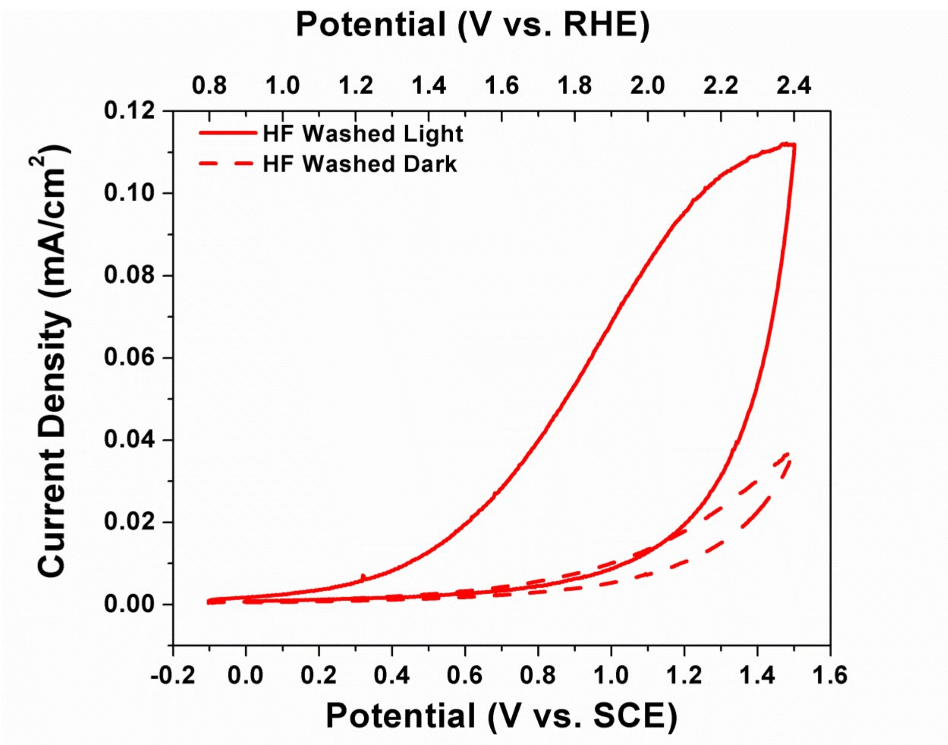

Fig S6- J-V forward and backward scans for H-terminated flat n-type silicon wafer for both light and dark conditions.

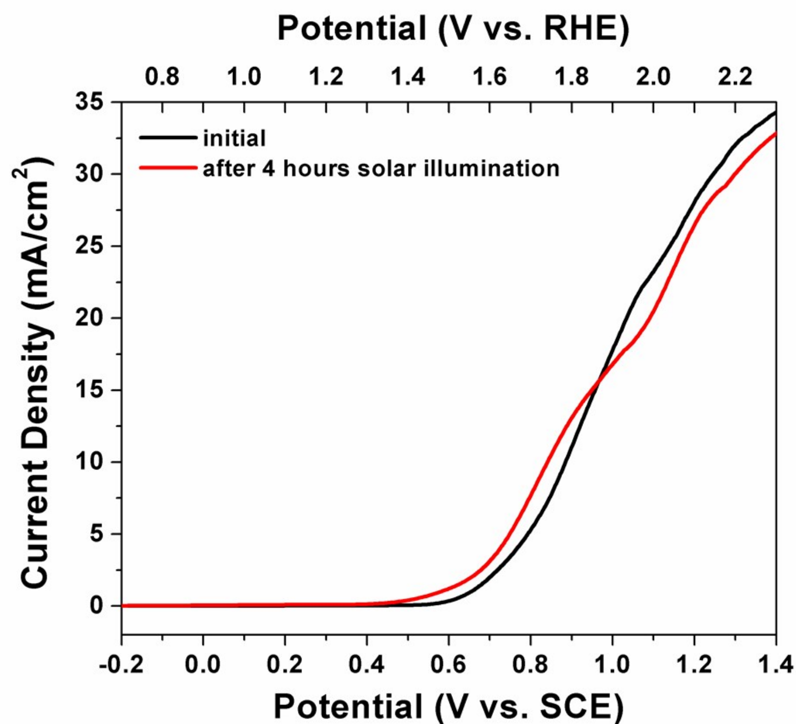

Fig S7- Stability test of C-Passivated (textured) silicon photoanode. This is achieved through continuous illumination of C-passivated nanotextured silicon electrodes for duration of 4 hours. Whereas a slight decrease in current density is observed in J-V scans, this indicates these devices to exhibit stability under this condition.

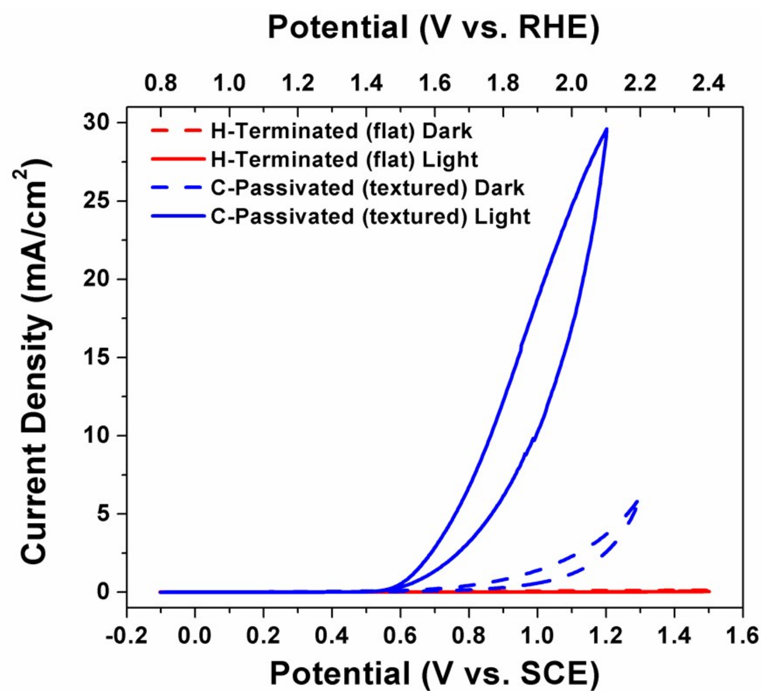

Fig S8- J-V forward and backward scans for all sample types shown in the main text.

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