Supplementary Information: Orientation dependence of the pseudo-Hall effect in p-type 3C-SiC four terminal device under mechanical stress

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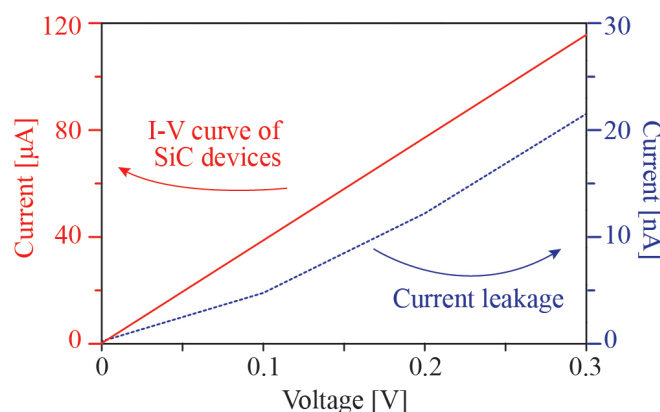## 1   Current-Voltage characteristic of the fabricated devices

Fig. 1 The current-voltage characteristic of a four terminal device and the leakage current through the SiC/Si heterojunction.

The current-voltage (I-V) characteristics of the SiC four terminal resistors were performed using HP4145B. Figure 1 shows the I-V curve of a four terminal device and the leakage current through the SiC/Si hetero-junction. Due to the discontinuity of the energy bands of SiC and Si, current is blocked from flowing through the SiC layer to the Si substrate. The ratio of the leakage current to the current through the four terminal device is below 0.02 %, indicating that Si did not contribute to the measured data.

2   The change of the offset voltage in a SiC four terminal device under several loading cycles

Figure 2 shows the generated voltage of sample A under a constant applied current of $10\,\mu$A for several loading cycles. This result indicated the excellent reproducibility of the output voltage without any significant drift.

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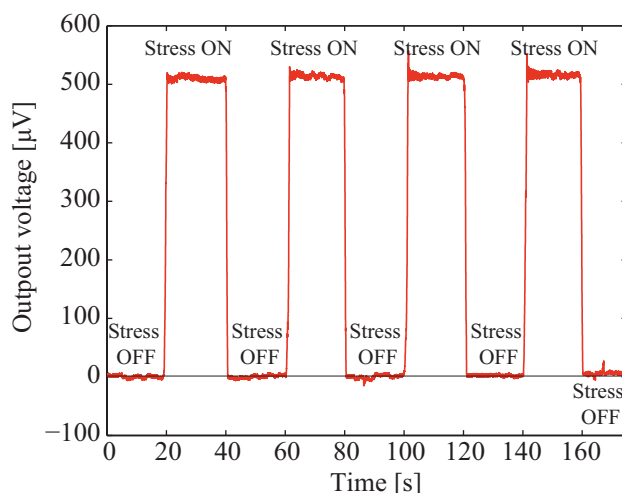[b] *School of Engineering, Griffith University, Queensland, Australia.*

Fig. 2 The offset voltage between terminals 3 and 4 under several loading cycles (the applied stress was 264 MPa).

3 The deduction of the stress tensors and piezoresistive coefficients

3.1 Stress tensors

The ratio of the generated voltage (V_{out}) across terminals 3 and 4 to the applied voltage across terminals 1 and 2 (V_{in}) under stress can be quantified by the coefficients π_{61}, π_{62}, π_{63}, π_{64}, π_{65} and π_{66}, as expressed in the following equation[1]:

$$V_{out} = V_{in}(\pi_{61}\sigma_1 + \pi_{62}\sigma_2 + \pi_{63}\sigma_3 + \pi_{64}\sigma_4 + \pi_{65}\sigma_5 + \pi_{66}\sigma_6) \tag{1}$$

where σ_i (i varying from 1 to 6) are the components of the stress tensors. For the case of a thin film semiconductor, the components related to the out-of-plane axis (π_{63}, π_{64}, and π_{65}) are negligible. Therefore, the ratio of the generated voltage (V_{out}) across terminals 3 and 4 to the applied voltage across terminals 1 and 2 (V_{in}) is[2]:

$$V_{out} = V_{in}(\pi_{61}\sigma_1 + \pi_{62}\sigma_2 + \pi_{66}\sigma_6) \tag{2}$$

Let β be the angle between the direction of the current and applied stress, the normal stresses and shear stress can be obtained using Mohr's circle, as shown in Fig. 3. Accordingly, the stress tensors are[3]:

$$\begin{cases} \sigma_1 = \sigma\cos^2\beta \\ \sigma_2 = \sigma\sin^2\beta \\ \sigma_6 = -\dfrac{\sin 2\beta}{2}\sigma \end{cases} \tag{3}$$

3.2 Equation of piezoresistive coefficients

The piezoresistive coefficients π_{61}, π_{62}, and π_{66} are[2]:

$$\begin{cases} \pi_{61} = a(l_1^3 l_2 + m_1^3 m_2 + n_1^3 n_2) \\ \pi_{62} = -a(l_1^3 l_2 + m_1^3 m_2 + n_1^3 n_2) \\ \pi_{66} = b + 2a[(l_1 l_2)^2 + (m_1 m_2)^2 + (n_1 n_2)^2] \end{cases} \tag{4}$$
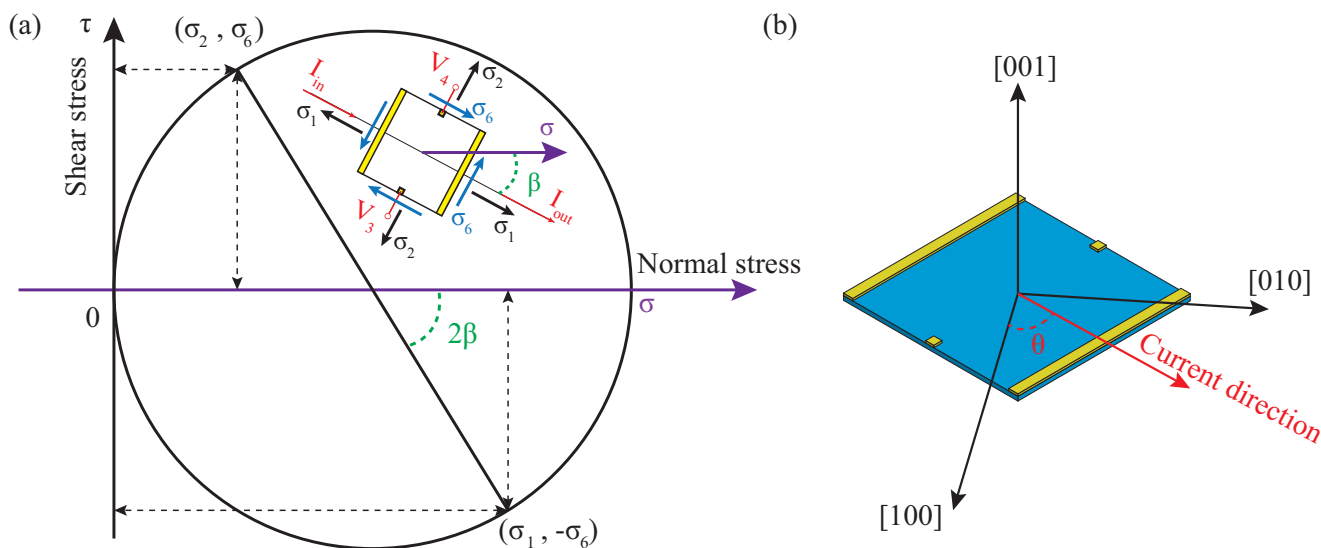
Fig. 3 The Mohr's circle used to calculate the stress tensors applied to four terminal devices.

here, l_i, m_j, and n_k are direction cosines[4]. In (100) plane, when the coordinates rotate about [001] axis an angle of θ, the matrix $[l_i \ m_i \ n_k]$ is[4]:

$$[l \ m \ n] = \begin{bmatrix} \cos\theta & \sin\theta & 0 \\ -\sin\theta & \cos\theta & 0 \\ 0 & 0 & 1 \end{bmatrix}. \tag{5}$$

Substitute Eq. 5 into Eq. 4, we have:

$$\begin{cases} \pi_{61} = -a\dfrac{\sin 4\theta}{4} \\ \pi_{62} = a\dfrac{\sin 4\theta}{4} \\ \pi_{66} = b + a\sin^2 2\theta \end{cases} \tag{6}$$

From Eq. 2, Eq. 3 and Eq. 6, the ratio of the output voltage (V_{out}) and the input voltage (V_{in}) per unit applied stress is:

$$\frac{V_{out}}{V_{in}} = \pi_{61}\sigma_1 + \pi_{62}\sigma_2 + \pi_{66}\sigma_6 = [-\frac{a}{4}\sin 4\theta \cos^2\beta + \frac{a}{4}\sin 4\theta \sin^2\beta - \frac{1}{2}(b + a\sin^2 2\theta)\sin 2\beta]\sigma \tag{7}$$

References

1 D. V. Dao, T. Toriyama, J. Wells, and S. Sugiyama, *Sens. Mater.*, 2002, **15**, 113-135.
2 Y. Kanda, *Jpn. J. Appl. Phys.*, 1987, **26**(7R), 1031.
3 R. C. Jaeger and J. C. Suhling, *IEEE T. Compon. Hybr.*, 1993, **16**, 925.
4 Y. Kanda, *IEEE Transactions on electron devices*, 1982, **29**(1), 64-70.