Supporting Data

Figure A.1. (A) Anodic etching processes for obtaining etched-Si with frameworks in ultranano scale. (B) The top view of etched-Si flakes (C) The bottom view of etched-Si flakes.

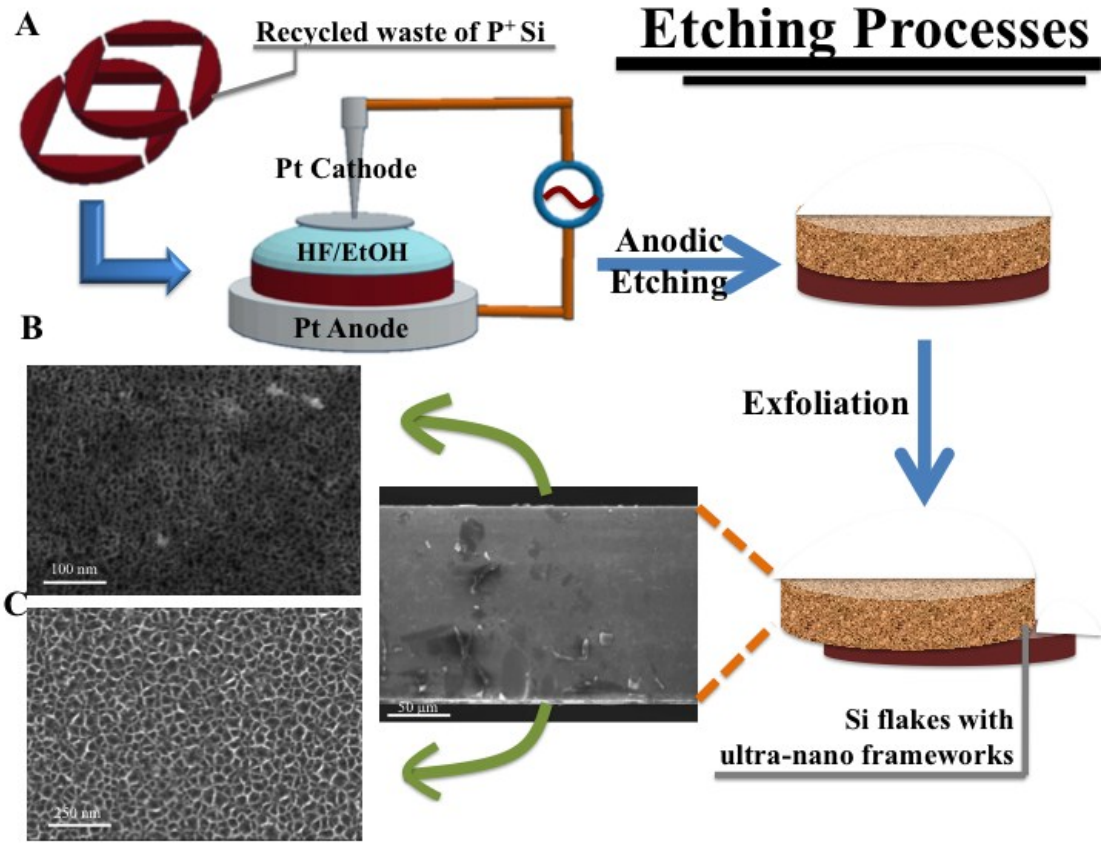

Figure A.2. (A) The full XPS spectrum of SiUPs. (B) The high-resolution scanning spectra of O 1s core-level XPS SiUPs.

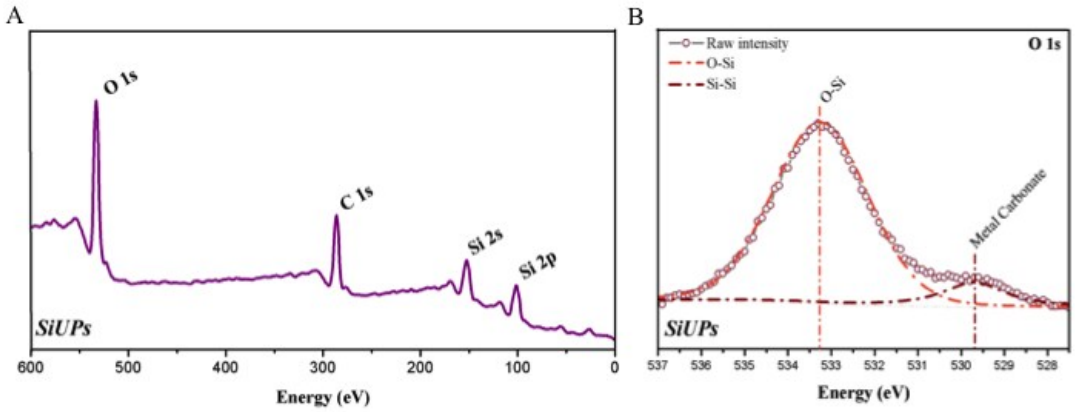

Figure A.3. (A) Optical images of SiUPs, r-Si, and c-Si. (B) The high-resolution O 1s XPS spectrum of SiUPs.

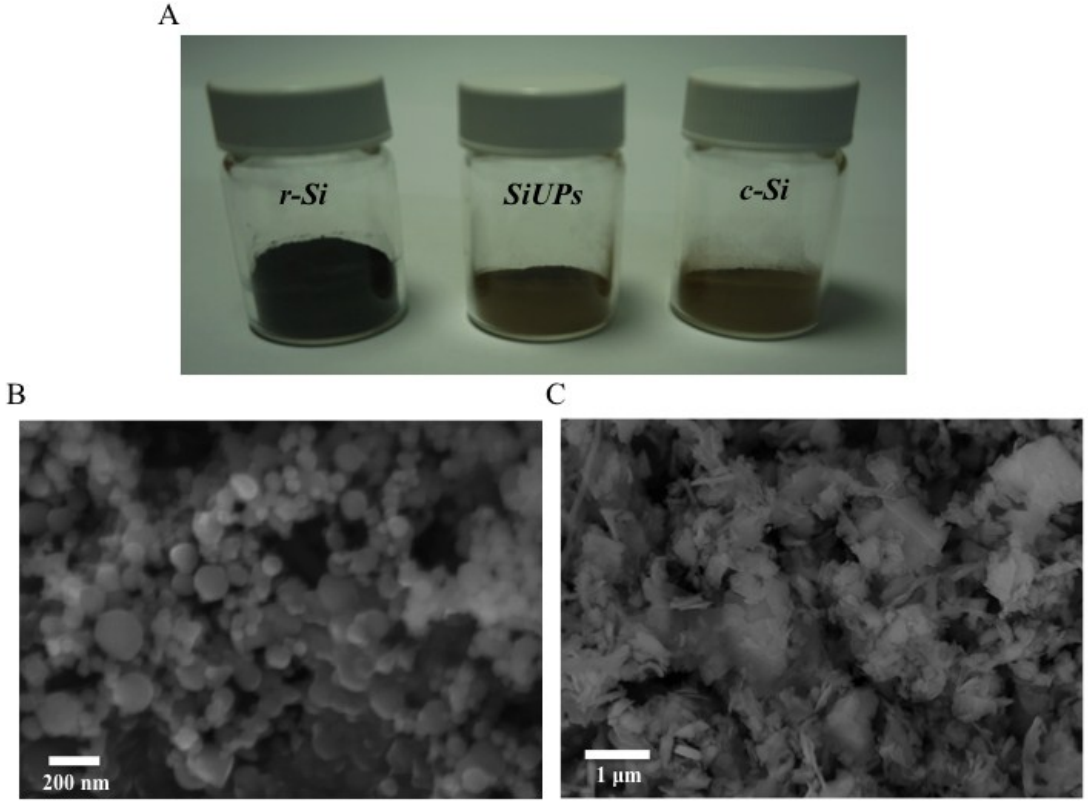

Figure A.4. TEM images of TD-SiUPs-31 and m-SiUPs

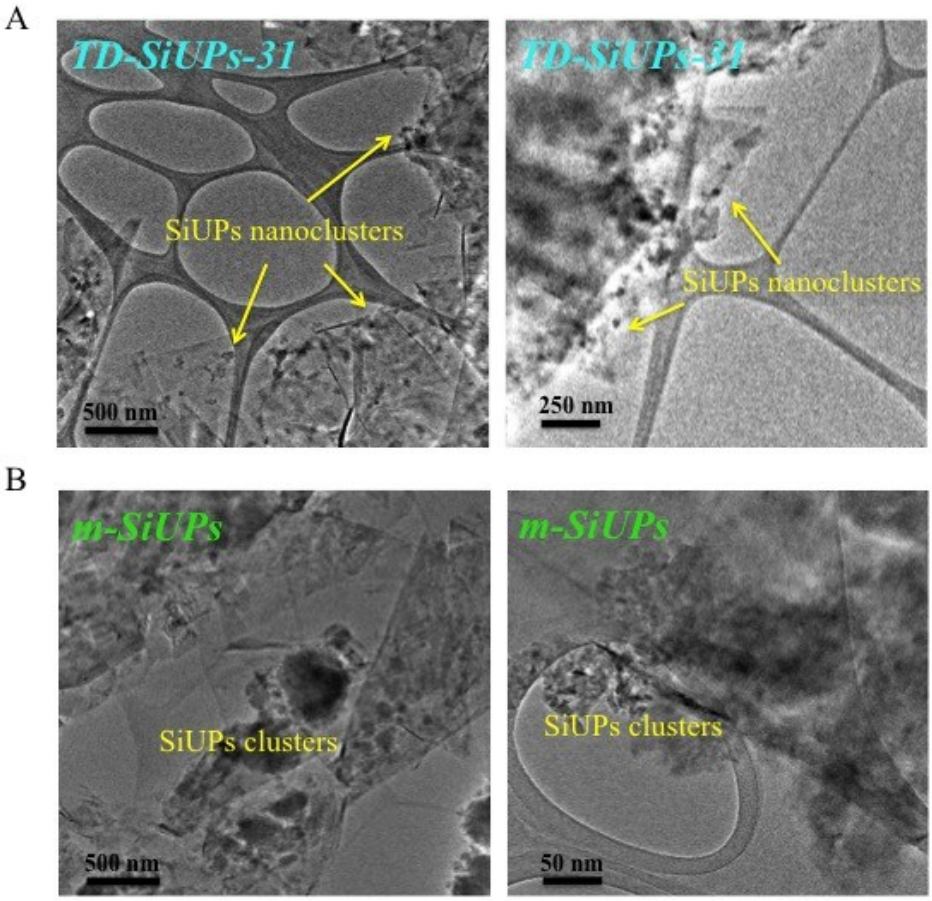

Figure A.5. Low-magnification SEM images of TD-SiUPs-31 and m-SiUPs.

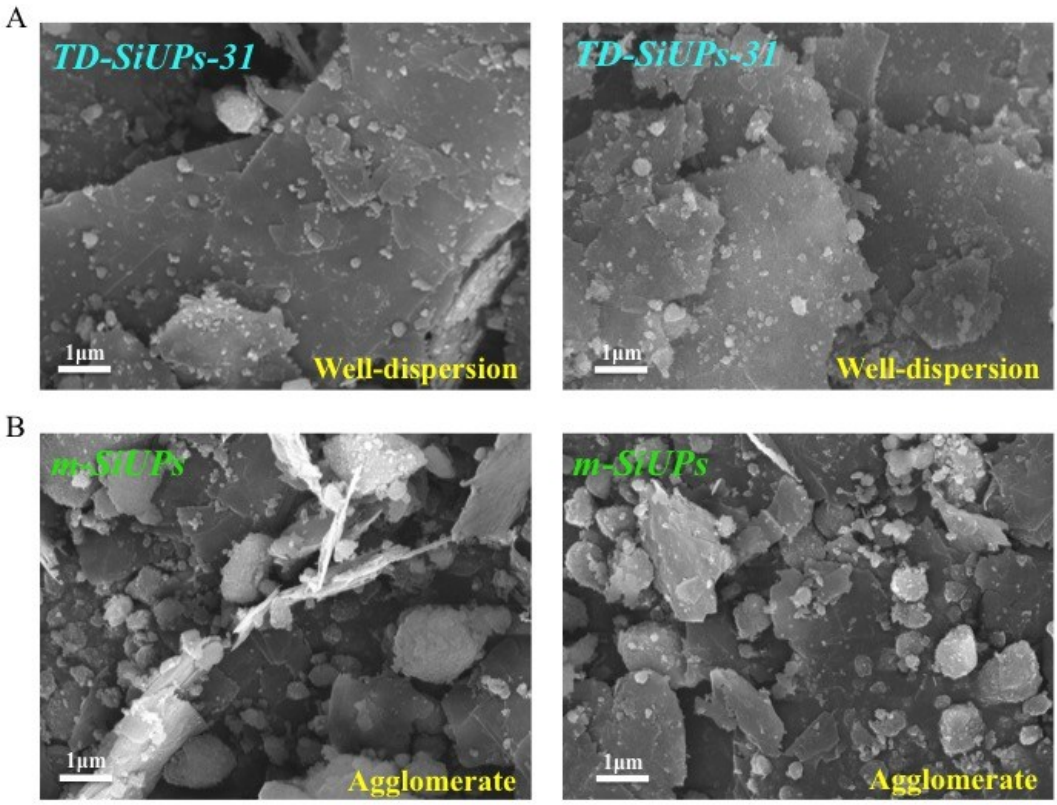

Figure A.6. BET analysis of TD-SiUPs-31 and m-SiUPs.

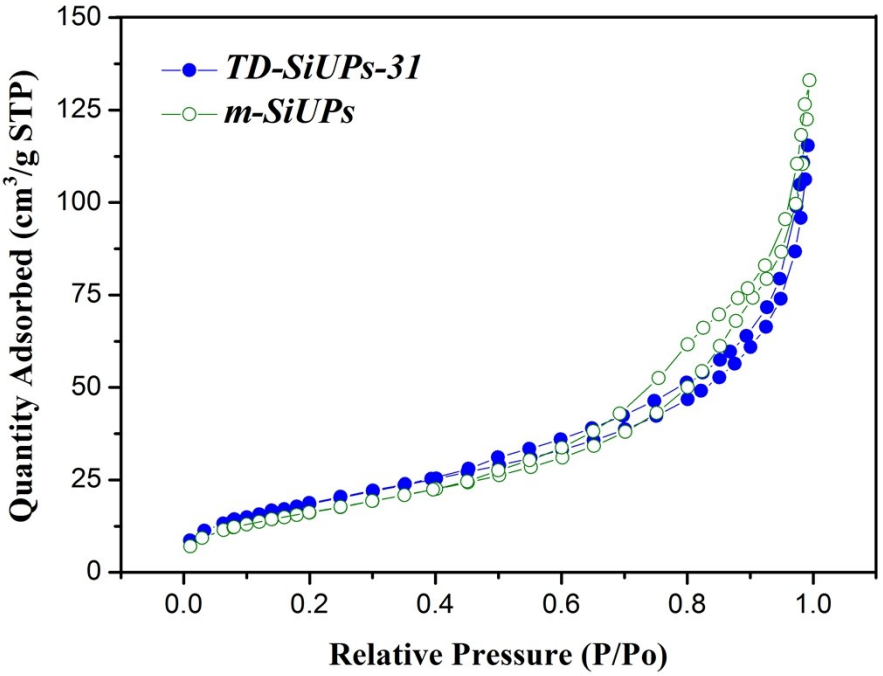

Figure A.7. (A) Cycling performance of graphitic flakes at two current densities of 0.2 and 0.8 A g^{-1} for 100 cycles. (B) The rate performance of graphitic flakes at different current densities.

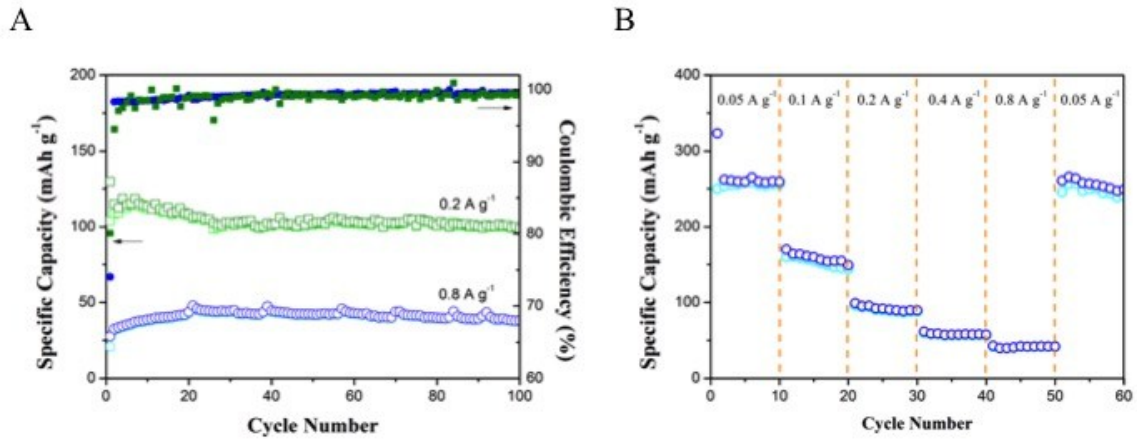

Figure A.8. Exhibited Coulombic efficiency of (A) TD-SiUPs-11 and (B) TD-SiUPs-23.

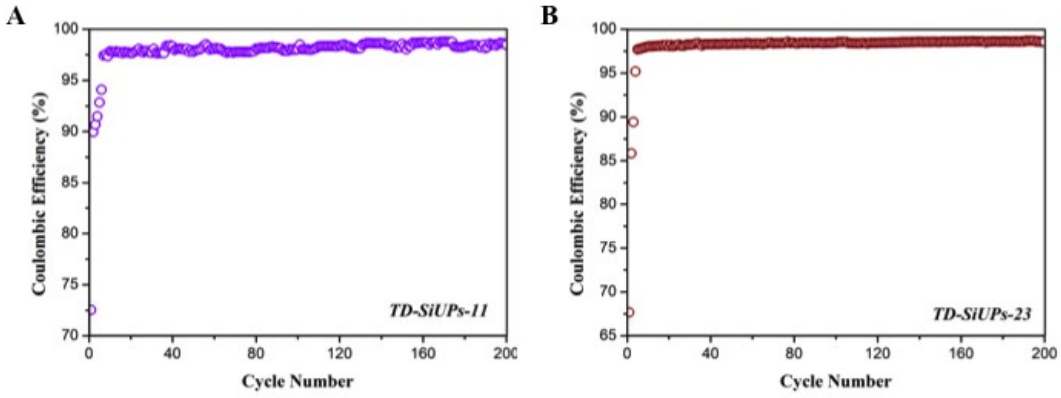

Table A.1. The summary of characteristics for SiUPs, c-SiNPs, and r-SiNPs.

Sample	Diameters [nm]	100^{th} cycle discharged capacity [mAh g^{-1}]	Capacity retention after 100 cycles [%]	Cost
SiUPs	<10	602.3	19.94	Low
c-SiNPs	40~200	31.2	1.02	High
r-SiNPs	50~1000	18.7	0.74	Low