

Electronic Supplementary Information

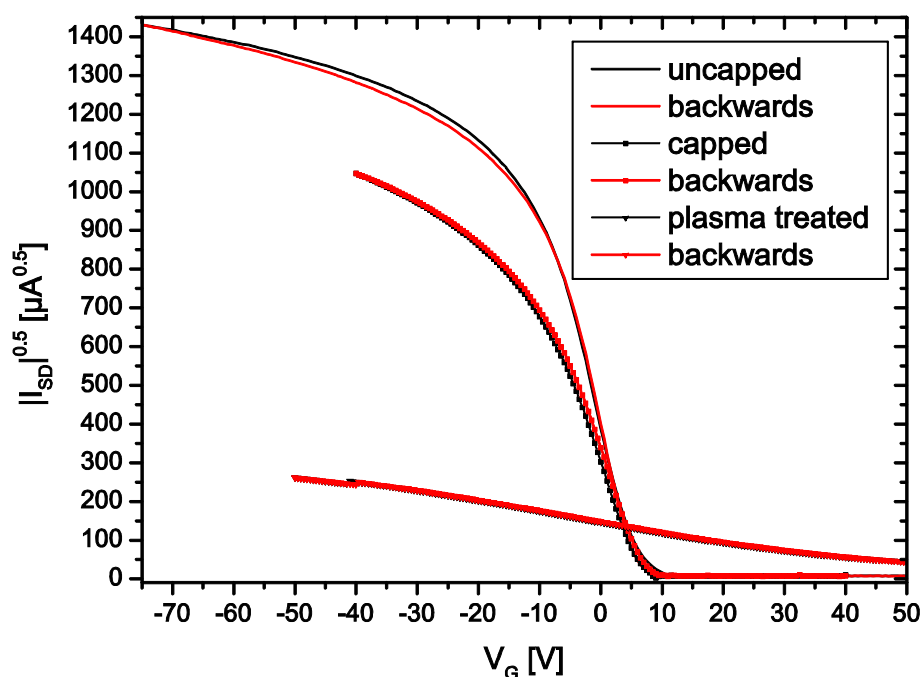
Urea detection in buffer solution with organic field effect transistors and a semipermeable membrane as top gate dielectric

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Evaluation of parylene-C as top-gate dielectric:

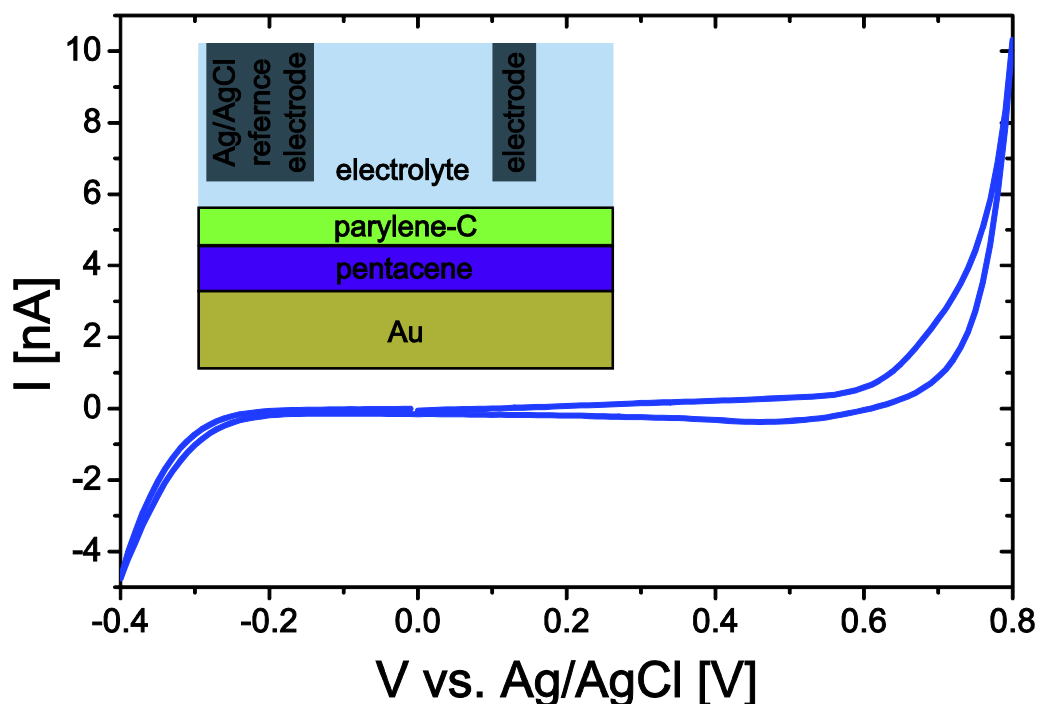
In prior experiments, we have identified tetratetracontane (TTC), a paraffin wax, as possible encapsulation material¹. The main problem of the wax is that it is rather fragile, thus the long term stability is limited. A polymer layer of cross linked parylene-C has much better mechanical stability.

For this optimization process, double gate OFETs were produced: Gate electrodes were patterned via a Lift-Off process: 15 nm of Au were deposited followed by 6 nm of Al and the Lift-Off was performed with 1165 Remover. An etch stop mask was defined from ma-P 1275 developed with ma-D 331 on the gate contact pads. Subsequently, nominally 1.7 μm parylene-C were deposited as the bottom gate dielectric. The thickness of the parylene layer was measured on glass slides using UV-VIS spectroscopy from the distance of the minima in transmission. An etch mask was fabricated on top of the bottom gate dielectric using again ma-P 1275 and the parylene-C dielectric layer patterned by reactive ion etching (RIE) in a parallel plate RIE chamber with a power of 200 W and 50 sccm O_2 . Onto an OFET with pentacene as the organic semiconducting layer (13 nm of pentacene, Sigma 698423, purified by one sublimation run by CreaPhys GmbH), we deposited 100 nm parylene-C. This layer deposition caused some minor damage to the organic semiconducting film², see also **Fig. S1**.



Supporting Figure S1: Evolution of a pentacene transistor after capping and oxygen plasma treatment. The source drain voltage was -0.3 V.

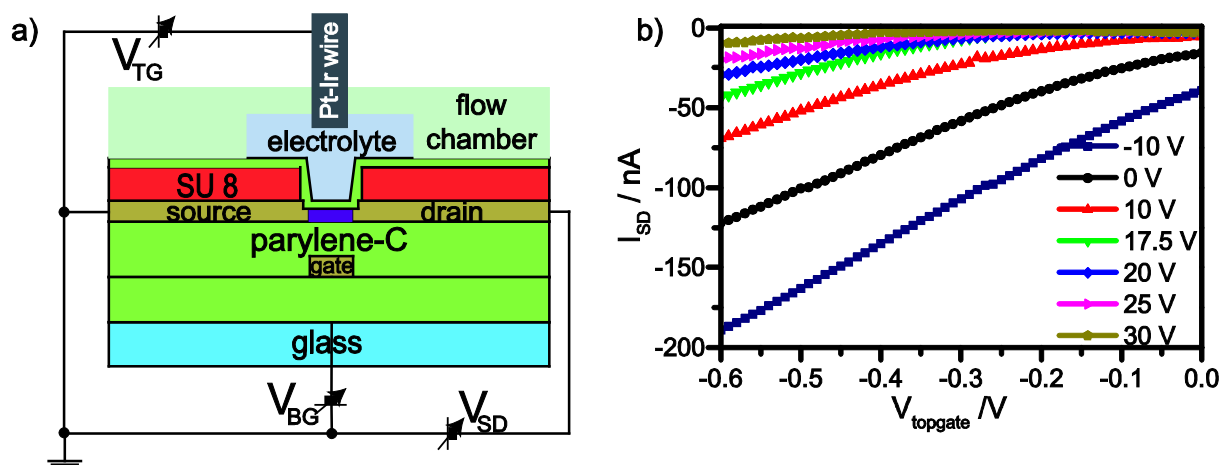
To evaluate the sealing properties of the parylene coating, we deposited a 14 nm thick pentacene film onto an Au electrode and encapsulated it with a thin parylene layer. The pentacene oxidation/reduction peak, which is a major contribution to Faradaic currents in bare pentacene films, was absent in cyclic voltammetry experiments with encapsulated films (see **Fig. S2**). This showed that the passivation layer prevents charge transport between pentacene and the electrolyte.



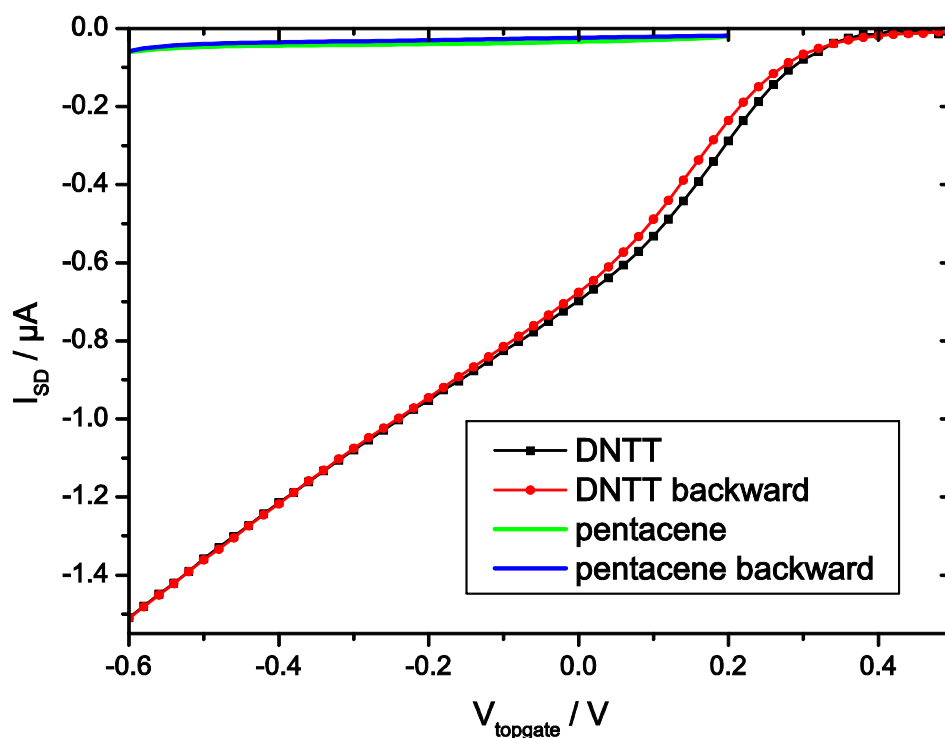
Supporting Figure S2: *Cyclic Voltammetry of capped pentacene layer. Cyclic voltammetry of a pentacene layer capped with parylene-C on the Au working electrode in a three electrode setup. Ag/AgCl was the reference electrode and a Pt electrode the counter electrode. The electrolyte was 10 mM DPBS. The measurement was performed using an Ivium CompactStat.*

Next, we used a thin parylene-C layer as the top gate dielectric to fabricate Double Gate Organic Field Effect Transistors (DG-OFETs). The top gate was a Pt/Ir wire in 10 mM Dulbecco's phosphate buffered saline (DPBS) electrolyte buffer. For this purpose, the sample was glued in a commercial flow chamber. Since the nominal thickness of the organic semiconductor was below 20 nm, we expected it to be below Debye length.³ In this case, the advantage of the DG-OFET geometry is that the top gate threshold voltage can be adjusted by the bottom gate voltage in order to maximize the transconductance for the top gate.⁴ This behavior is confirmed in **Fig. S3 b**.

Here, the threshold voltage of the top gate was shifted by 0.2 V, when the bottom gate voltage change was 10 V. This proved that a thin parylene-C layer is suited as a top gate dielectric layer. Pentacene is known to oxidize in the presence of oxygen⁵ therefore it is no surprise that the OFETs based on pentacene did not stand oxygen plasma treatment for the attachment of urease (see **Fig. S1**). Therefore we replaced pentacene with Dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNNTT), an oxygen stable organic semiconductor⁶ to maintain transistor performance upon plasma treatment (see **Fig. S4**).

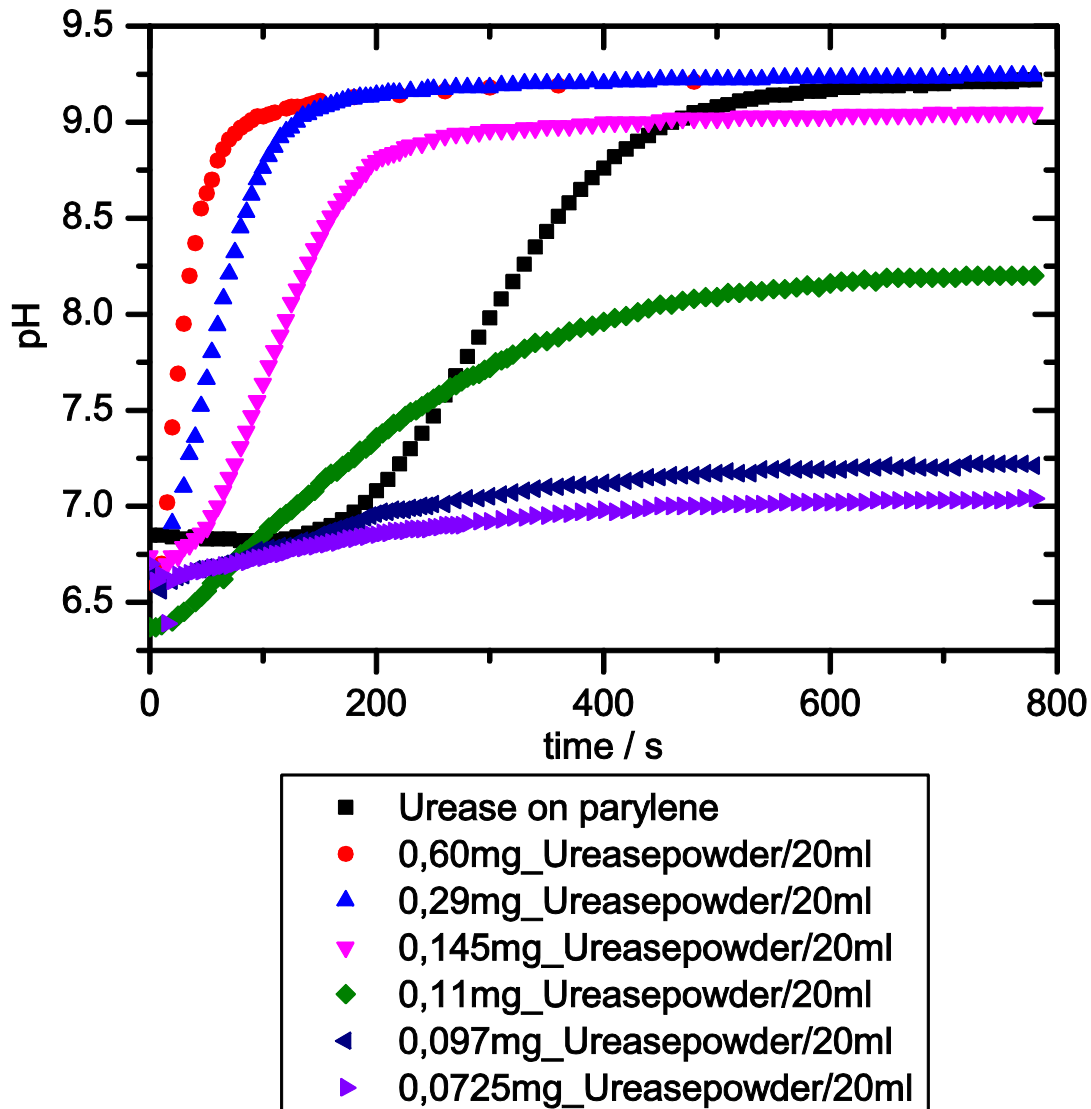


Supporting Figure S3: a) Schematic of the device architecture and measurement scheme for the characterization of the DG-OFETs in solution. b) Top gate transconductance curve with different bottom gate voltages applied as indicated in the graph at $V_{SD} = -0.3$ V.



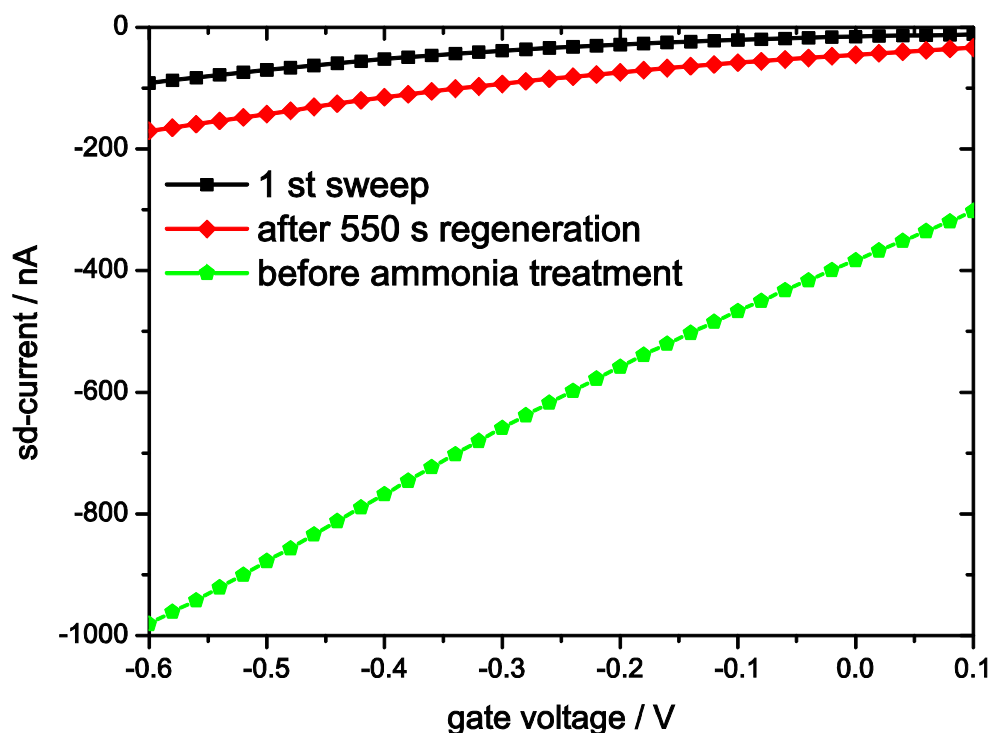
Supporting Figure S4: Comparison between electrolyte gated sweeps of a plasma treated pentacene transistor and a DNTT based one, which was fully functionalized, at $V_{SD} = -0.3$ V. While the degradation of pentacene during the oxygen plasma treatment decreased the performance, the DNTT based transistor showed acceptable performance after the functionalization steps. The source drain current was corrected for leakage current through the electrolyte, which got non-negligible for positive gate voltages, as previously reported¹.

Urease activity evaluation:



Supporting Figure S5: pH measurement of urease activity in Milli-Q water without buffer. 20 ml of 10 mM urea solution dissolved in Milli-Q water were left to stabilize the pH value. Then the indicated amount of urease or a functionalized parylene coating were added to the solution and the evolution of the pH value in time was recorded.

OFET current regeneration after exposure to ammonia:



Supporting Figure S6: Regeneration of transistor current in 10 mM DPBS after ammonia treatment. After exposure to ammonia solution, the electrolyte was replaced with fresh 10 mM DPBS buffer and transistor sweeps recorded at $V_{SD} = -0.3$ V and floating bottom gate. For comparison, the original transistor curve is added.

Supplementary Information References:

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4. H. K. Lim and J. G. Fossum, *Ieee Transactions on Electron Devices*, 1983, **30**, 1244-1251.
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6. T. Yamamoto and K. Takimiya, *Journal of the American Chemical Society*, 2007, **129**, 2224-2225.