Electronic Supplementary Material (ESI) for Journal of Materials Chemistry C.

(Supporting Information)

A Robust Ionic Liquid – Polymer Gate Insulator for High-Performance Flexible Thin Film Transistors

Jieun Ko,[a] Su Jeong Lee,[b] Kyongjun Kim,[a] EungKyu Lee,[a] Keon-Hee Lim,[a] Jae-Min Myoung,[b] Jeeyoung Yoo,*[a] and Youn Sang Kim*[a, c]

[a] Program in Nano Science and Technology, Graduate school of Convergence Science and Technology, Seoul National University, Seoul, 151-744, Republic of Korea

[b] Department of Advanced Materials Engineering, Yonsei University, Seoul 120-749, Republic of Korea

[c] Advanced Institutes of Convergence Technology, 864-1 Iui-dong, Yeongtong-gu, Suwon-si, Gyeonggi-do 443-270, Republic of Korea

Contents

1. Experimental procedure

Preparation of the dielectric layer and semiconductor layer solution

To prepare an ionic liquid - polymer (IL-PVP) solution, poly(4-vinylphenol) (PVP) [Sigma Aldrich, M_w ~25,000], 4,4'-(hexafluoroisopropylidene)diphthalic anhydride (HDA) [Sigma Aldrich, 99%] and propylene glycol monoethyl ether acetate (PMGEA) [Sigma Aldrich, ≥ 99.5%] were mixed in a weight ratio of 10 : 1 : 56. The PVP solution was stirred for 12 hr vigorously. Since the ionic liquids are sensitive to water, 1-ethyl-3-methylimidazolium bis(trifluoromethylsylfonyl)imide (EMIM-TFSI) [Sigma Aldrich, ≥ 98%] was stored in vacuum oven at 70 ^{o}C for 12 hr before use to remove minimum moisture. The dried EMIM-TFSI was added to PVP solution in a 1:1 weight ratio with PVP:EMIM-TFSI. The ionic liquid - polymer solution was stirred for 12 hr vigrously in ambient condition. The semiconductor solution was prepared by dissolving 0.001 mol of zinc oxide (ZnO) [Sigma Aldrich, 99.99%] into 12 ml of ammonium hydroxide [Alfa Aesar, 25 wt% NH_3 in water, 99.99%]. The ZnO solution was refrigerated for 5 hr until obtain clear solution.

Fabrication of the MIM and TFT devices

To faricate the IL-PVP dielectric layer, the IL-PVP solution was spin-coated (30 s, 2000 rpm) onto substrates. The IL-PVP dielectric layer was dried in vacuum oven at 70 ^{o}C for 12 hr and annealed at 110 ^{o}C for 1 hr on hot plate in ambient condition. For metal-insulator-metal (MIM) devices, the IL-PVP dielectric layer was prepared onto a heavily boron-doped P-type silicon (P^{++}-Si) (100) wafer and an aluminum (Al) electrode was deposited on the dielectric layer by thermal evaporation with 100 nm thickness. For the bottom-contact top-gate (BCTG) TFT, the semiconductor solution was spin-coated (30 s, 3000 rpm) on the UVO treated (30 min) thermal grown 200 nm SiO_2 wafer and annealed at 300 ^{o}C for 1 hr. After annealing, the Al source/drain electrodes (W/L : 1000/50 μm, thickness : 100 nm) were deposited onto the semiconductor layer by thermal evaporation with SUS masks. The IL-PVP dielectric layer was coated (30 s, 2000 rpm) on the source/drain and dried at 70 ^{o}C for 12 hr in vacuun oven. To obtain the source/drain contact area, the IL-PVP dielectric layer on source/drain was cleaned off with cotton swab and solvent, acetone or PGMEA. Then the dielectric layer was annealed at 110 ^{o}C for 1 hr on hot plate. Finally, the silver (Ag) gate electrodes (thickness: 100 nm) were evaporated on the dielectric layer by thermal evaporation with SUS masks. For the flexible ZnO TFT, the ZnO solution was spin coated (30 s, 3000 rpm) on metal oxide treated PI film [Al_2O_3 (thickness: 20 nm) deposited on PI] and annealed at 300 ^{o}C for 40 min. After that, same procedure with preparation of the TFT was performed.

Characterization of the capacitance and TFT

The capacitance of the IL-PVP dielectric layer was measured using an Agilent 4284A 1kHz precision LCR meter. The current-voltage (I-V) measurements were performed using an Agilent 4155B semiconductor parameter analyzer. The impedance measurements were taken by an electrochemical analyzer (CHI660E: CH Instruments, Inc.). The elastic modulus was characterized by Nano Indentation System (Nano Indenter XP: MTU). The electrical measurements were performed in ambient environment conditions. The thermal behavior of the IL-PVP dielectric layer was characterized by thermo-gravimetric and differential scanning calorimetry (TG-DSC; Q5000 IR: TA) in air condition. The chemical characteristics of the IL-PVP dielectric layer was measured by attenuated total reflectance Fourier transform infrared spectroscopy (ATR-FT IR; Nicolet 5700: ThermoFisher). The thickness of the IL-PVP dielectric layers were characterized by surface profiler (Alpha-step IQ: KLA-Tencor). The morphology of the IL-PVP layer and semiconductor layer were investigated by atomic force microscopy (AFM; XE100: PSIA).

2. ATR-FT IR Analysis

Functional groups of cation		Functional groups of anion	
N=C-N stretching vibration	1560-1520 cm^{-1}	-CF_3 stretching	1350-1120 cm^{-1}
ring C=C vibration	1605-1585 cm^{-1}	asymetric vibration of CF_3	680-590 cm^{-1} 555-505 cm^{-1}
C-H vibration for cyclic cations	3172-3126 cm^{-1}	symetric vibration of CF_3	600-540 cm^{-1}

Table S1 Absorption peaks table of ATR FT-IR.

Reference

(1) Socrates G. *Infrared Characteristic Group Frequencies: Tables and Charts*, 3rd Edition, Wiley & Sons: New York, **2004**.

(2) Köddermann, T.; Wertz, C.; Heintz, A.; Ludwig, R. *ChemPhysChem* **2006**, 7, 1944-1949.

(3) Kiefer, J.; Fries, J.; Leipertz, A. *Appl. Spectrosc.* **2007**, 61, 1306-1311.

3. Impedance Analysis

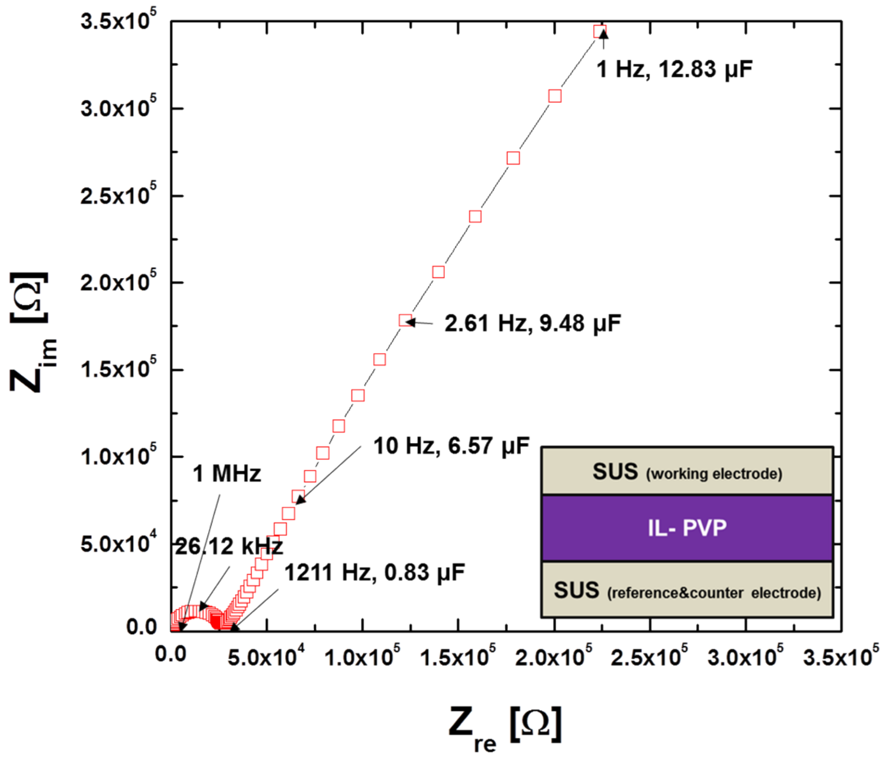

Figure S1 Nyquist plot of polymer insulator depending on frequency

Figure S1 shows a Nyquist plot including calculated capacitance value of each frequency. In this impedance analysis, SUS electrode was used as both working electrode and counter electrode. Frequency range of impedance analysis was 1 ~ 1 MHz. The area of SUS electrode was 1.76625 cm^2 and thickness of the IL-PVP layer was 300 μm. Amplitude of AC voltage was 5 mV and DC bias was not loaded. Since the Nyquist plot correspond to capacitive layer, bulk ionic conductivity of the IL-PVP layer was 49.2 μS/cm, and interfacial charge transfer conductivity was 0.636 μS/cm. Considering AC voltage amplitude and thickness of the IL-PVP, the capacitance of Figure 2b could be different from Figure 2a.

4. Nano Indenter Analysis

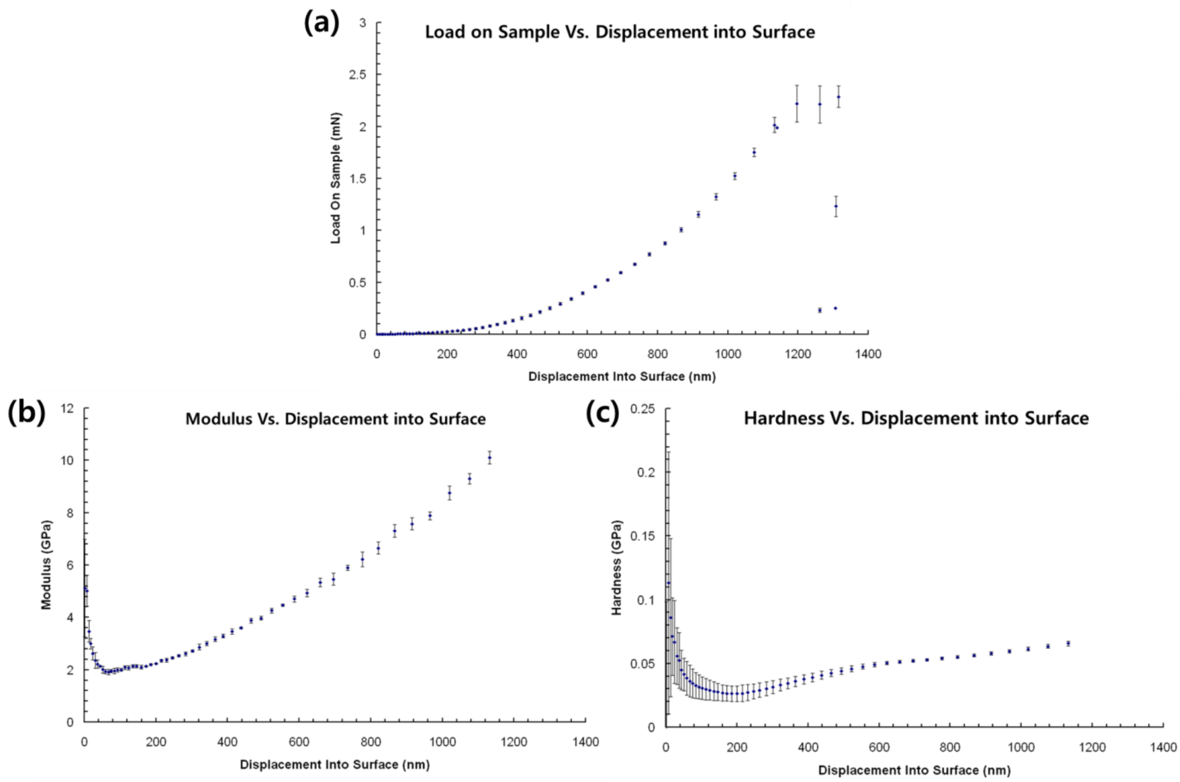

Figure S3 Nano-indentation analysis results of Load on sample (a), modulus (b), and hardness (c) versus displacement into surface. (scan rate: 10 nm/s, maximum indentation depth : 1000 nm, average result of 4 points).

5. AFM images of the IL-PVP and ZnO layer

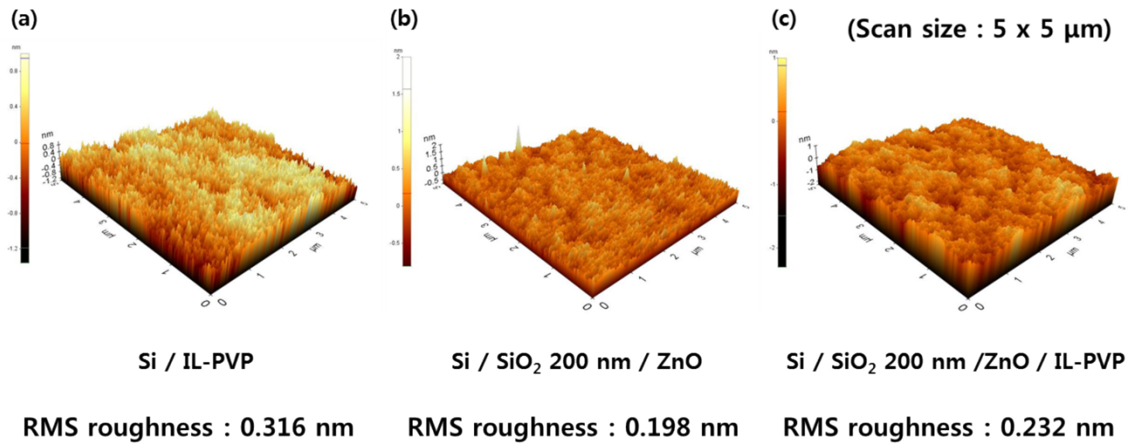

Figure S3 AFM images of the IL-PVP on a P^{++}-Si substrate (a), the ZnO on a SiO_2 200nm substrate (b), the IL-PVP on the ZnO layer which is coated on a SiO_2 200 nm substrate (c). (scan size: 1 X 1μm).

6. Hysteresis of the ZnO TFTs

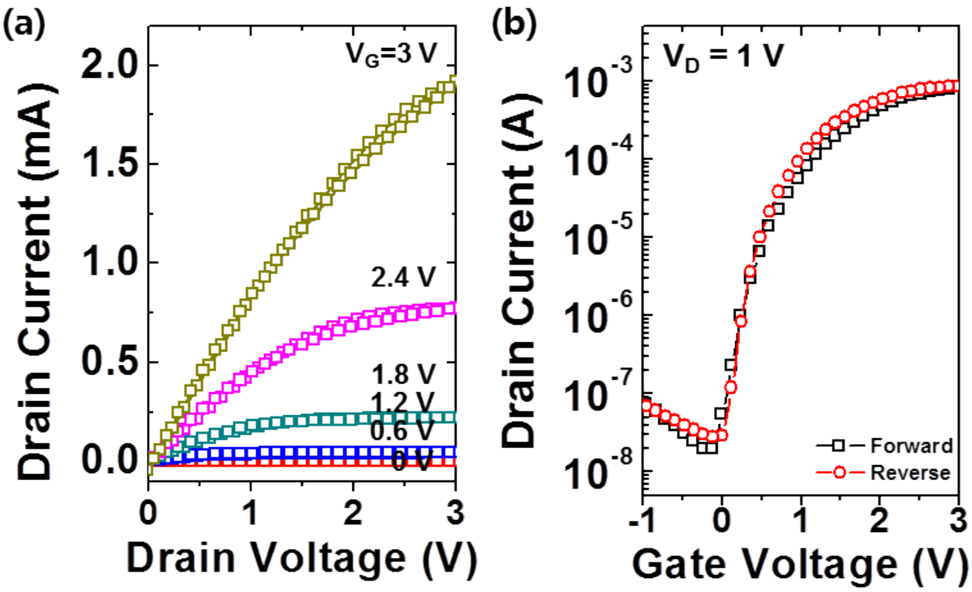

Figure S4 Output (a) and Transfer (b) hysteresis curves of the ZnO TFTs with the IL-PVP gate insulator.