

Electronic supplementary information

Transistor application of single crystals of [8]phenacene

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1. Lattice constants of phenacene crystals

Table S1 Lattice constants of phenacene crystals.

	a [Å]	b [Å]	c [Å]	β [°]	Ref.
Picene	8.472(2)	6.170(2)	13.538(7)	90.81(4)	18
[6]phenacene	12.130(1)	7.9416(7)	15.401(1)	93.161(8)	16
[7]phenacene	8.4381(8)	6.1766(6)	17.829(2)	93.19(1)	16
[8]phenacene	8.842(2)	6.043(1)	19.896(4)	92.92(3)	

2. FET parameters evaluated for each [8]phenacene single-crystal FET

Table S2 FET parameters of [8]phenacene single-crystal FETs with parylene-coated SiO₂ gate dielectrics.

sample	μ (cm ² V ⁻¹ s ⁻¹) ¹⁾	$ V_{th} $ (V)	ON/OFF	S (V/decade)	L (μ m)	W (μ m)
#1	1.0	31.3	2.3×10^8	1.4	30	1200
#2	1.0	33.4	1.0×10^6	2.8	30	1900
#3	1.3	19.1	2.1×10^8	4.4	50	200
#4	1.6	26.3	4.4×10^8	4.2	50	500
#5	1.6	31.7	4.7×10^8	1.4	50	600
#6	1.8	29.7	6.2×10^8	3.9	50	700
#7	1.5	27.8	4.5×10^8	4.4	50	600
#8	1.7	38.3	1.2×10^8	0.92	100	1400
#9	2.5	23.2	5.6×10^7	1.3	100	2100
#10	1.7	25.6	1.6×10^7	1.5	100	2300
#11	2.5	27.2	1.1×10^9	0.85	100	2300
#12	1.4	24.9	1.3×10^7	2.0	150	700
#13	8.2	28.1	3.5×10^8	1.6	450	900
#14	3.7	16.9	3.0×10^7	1.2	450	1700
#15	7.2	15.6	6.3×10^7	1.0	450	900
#16	7.5	18.4	3.9×10^7	1.2	450	600
#17	5.4	8.7	4.5×10^7	0.71	450	800
#18	6.0	34.2	4.5×10^7	1.2	450	1200
average	3(2)	26(8)	$2(3) \times 10^8$	2(1)		

Table S3 FET parameters of [8]phenacene single-crystal FETs with parylene-coated SiO₂ gate dielectrics, measured in four-terminal mode.

sample	μ (cm ² V ⁻¹ s ⁻¹)	$ V_{th} $ (V)	ON/OFF	S (V/decade)	L (μ m)	W (μ m)
#1	3.1	62.6	1.37×10^7	1.86	150	1700
#2	7.3	42.6	2.75×10^7	0.934	150	900
#3	6.3	36.0	2.14×10^7	1.14	150	800
average	6(2)	47(14)	$2.1(7) \times 10^7$	1.3(5)		

Table S4 FET parameters of [8]phenacene single-crystal FETs with parylene-coated PZT dielectrics.

sample	μ (cm ² V ⁻¹ s ⁻¹)	$ V_{th} $ (V)	ON/OFF	S (V/decade)	L (μ m)	W (μ m)
#1	2.02	3.5	6.2×10^2	2.8	100	200
#2	1.39	5.0	1.1×10^7	0.69	50	500
#3	2.07	4.9	9.2×10^6	0.40	100	700
#4	1.60	6.1	5.2×10^6	0.51	135	900
#5	1.16	3.8	5.3×10^3	1.8	100	600
average	1.6(4)	5(1)	$5(5) \times 10^6$	1(1)		

Table S5 FET parameters of [8]phenacene single-crystal FETs with EDL capacitors.

sample	μ (cm ² V ⁻¹ s ⁻¹)	$ V_{th} $ (V)	ON/OFF	S (V/decade)	L (μ m)	W (μ m)
#1	2.5×10^{-1}	2.427	2.13×10^2	4.8×10^{-1}	97	400
#2	3.5×10^{-1}	2.354	3.79×10^2	5.2×10^{-1}	100	800
#3	7.1×10^{-1}	2.366	2.18×10^7	8.3×10^{-2}	98	500
average	$4(2) \times 10^{-1}$	2.38(4)	$7(13) \times 10^6$	$4(2) \times 10^{-1}$		

3. L dependence of μ in [8]phenacene single-crystal FET with SiO_2 gate dielectric

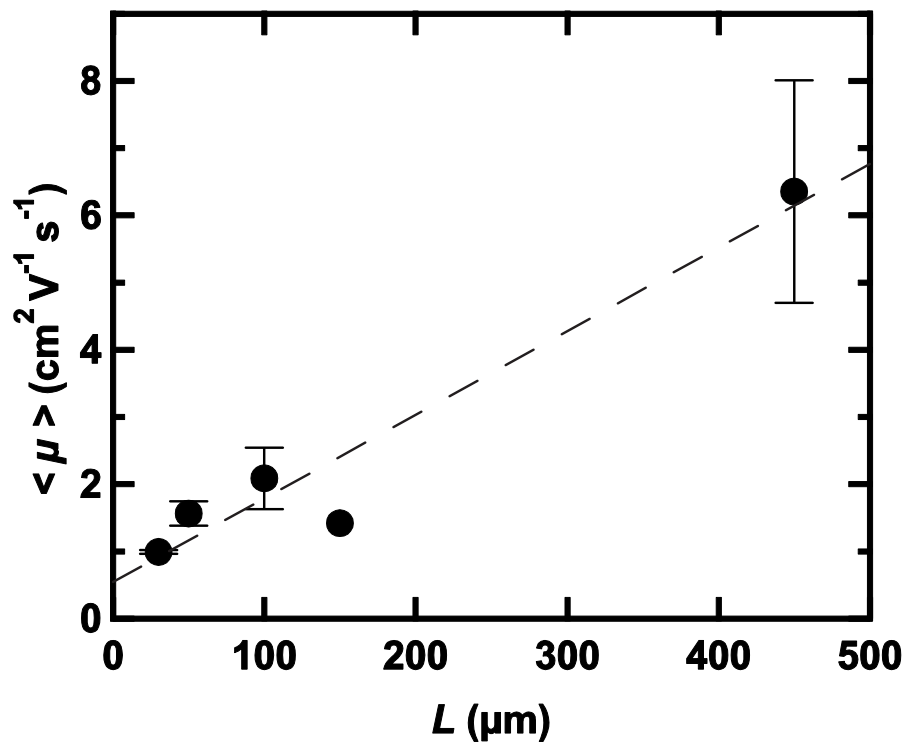


Fig. S1 Plot of $\langle \mu \rangle - L$ for an [8]phenacene single-crystal FET; dashed line represents best linear fit.

4. Transfer and output curves of [8]phenacene single-crystal FET with HMDS-coated SiO₂ gate dielectric

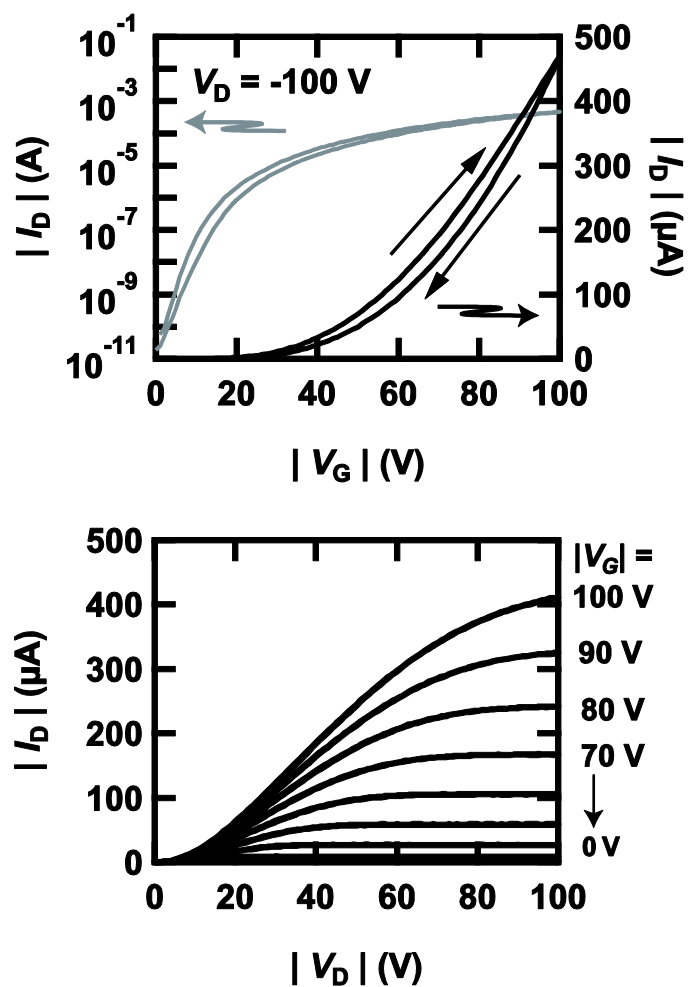


Fig. S2 Transfer (top) and output (bottom) curves of an [8]phenacene single-crystal FET with HMDS-coated SiO₂ gate dielectric.

5. Transfer and output curves of typical PDIF-CN₂ single-crystal FET

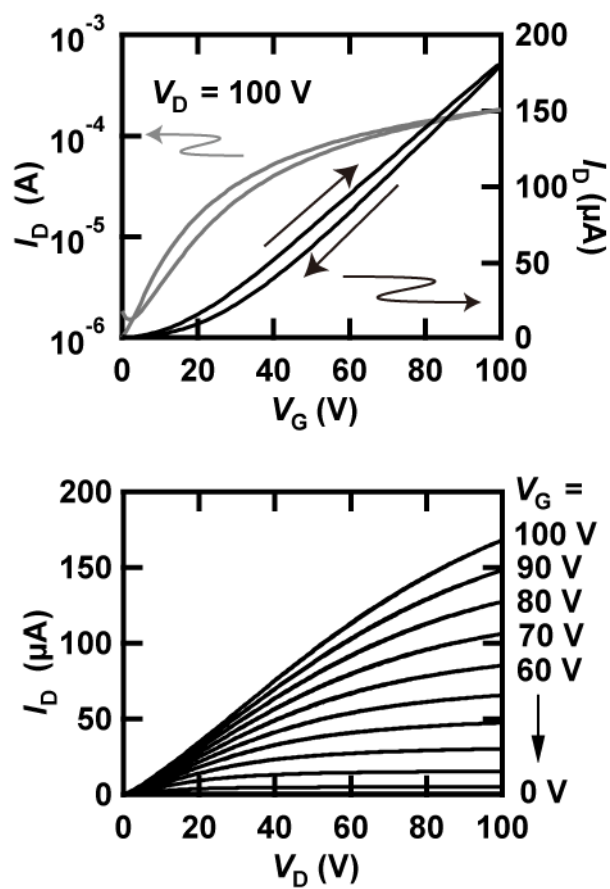


Fig. S3 Transfer (top) and output (bottom) curves of a PDIF-CN₂ single-crystal FET with parylene-coated SiO₂ gate dielectric.