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Supporting Information

Low Operating Voltage and Low Bias Stress in Top-Contact $SnCl_2Pc$/ CuPc Heterostructure based Bilayer Ambipolar Organic Field-effect Transistors

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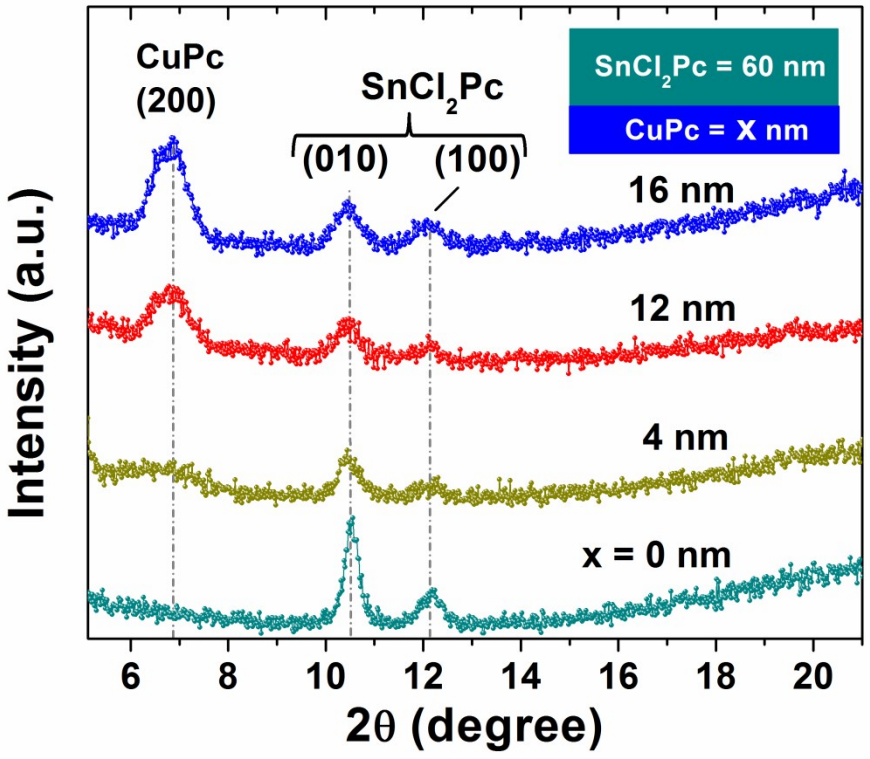

Fig. S1. X-ray diffraction (XRD) patterns of $SnCl_2Pc$ (60 nm) deposited on different thicknesses of CuPc layer at a subtatre temperature, T_d = 60 ºC. Inset shows a schemaic of the layer configuration (60 nm $SnCl_2Pc$ as top layer and CuPc with varying thickness as bottom layer) used for the XRD measurement.

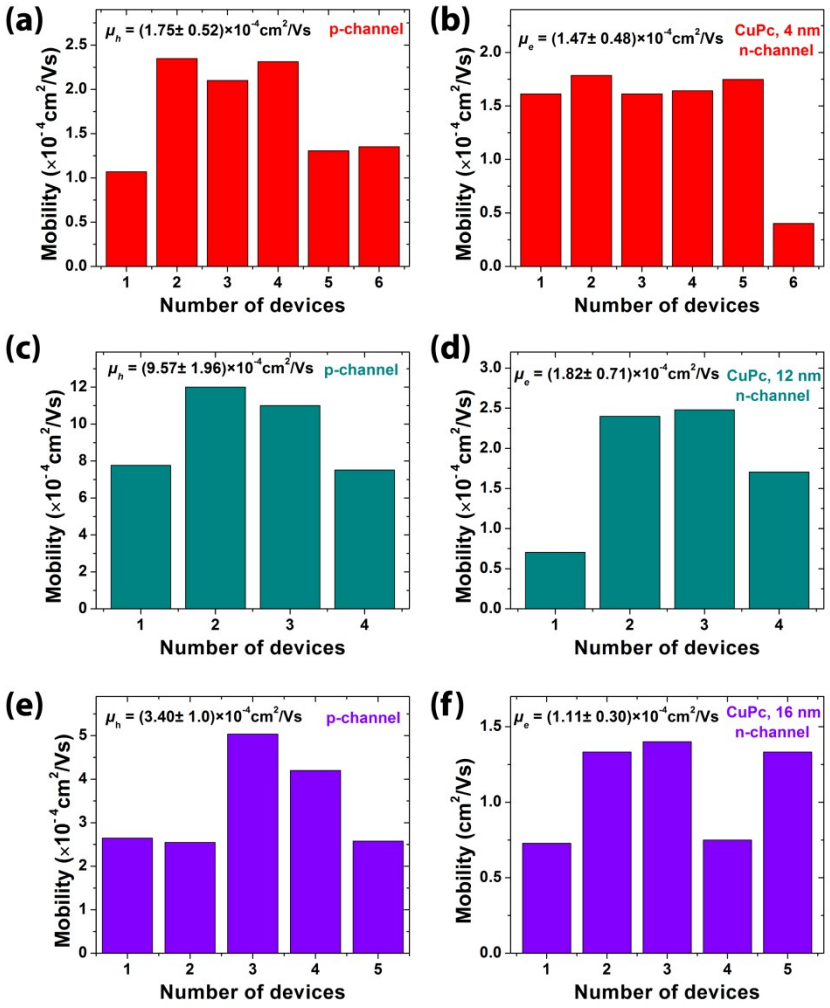

Fig. S2. The mobility (μ) distribution of representative devices for different thicknesses of CuPc layers for p-channel (left panel) and n-channel (right panel). Average μ and its standard deviation are mentioned in each case.

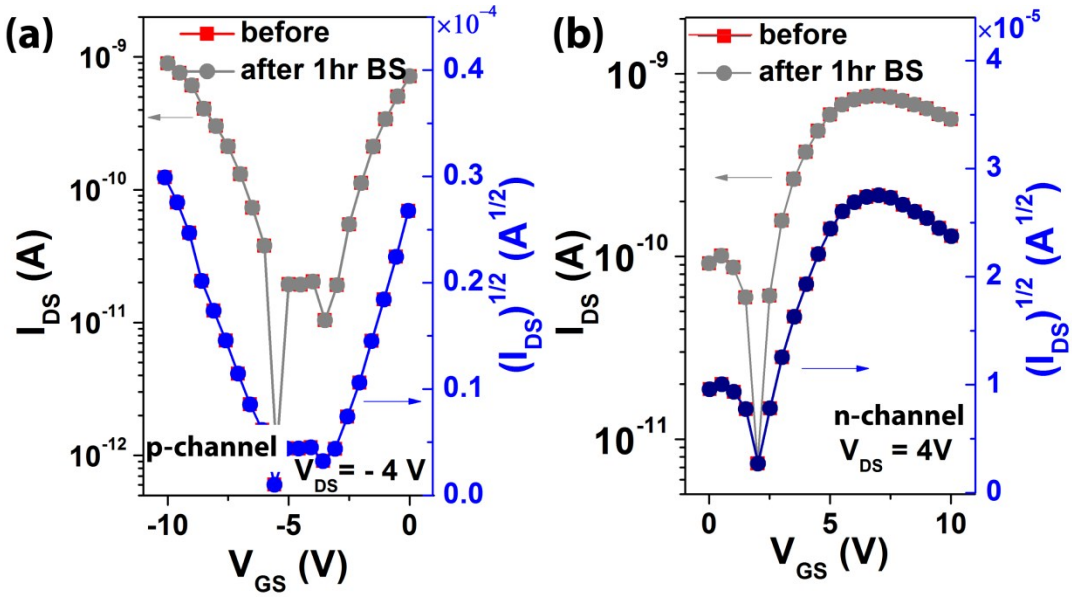

Fig. S3. Transfer characteristics of top-contact OFET with PMMA/Al_2O_3 bilayer dielectric at room temperature before and after an applied cyclic gate-bias stress (BS) for 1 hr in (a) p-channel of V_{GS} = -10 V(V_{DS} = - 4V) and (b) n-channel of V_{GS} = 10 V (V_{DS} = 4 V) devices.

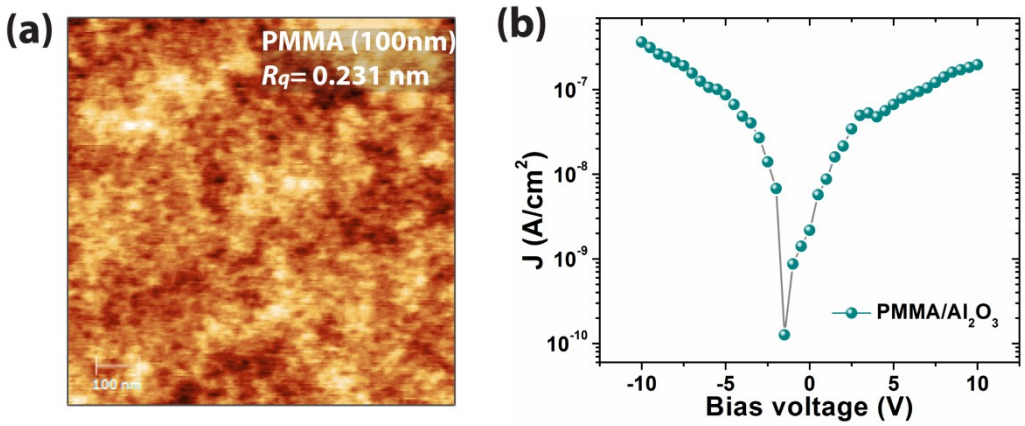

Fig. S4. (a) AFM image of PMMA layer. Surface roughness (R_q) is shown as inset. (b) Leakage-current density (J) as function of bias voltage for PMMA (100 nm)/Al_2O_3 (15 nm) bilayer gate dielectric.