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Supporting Information

Impact of Atomic Layer Deposited SiO_2 Passivation for High-k $Ta_{1-x}Zr_xO$ on InP Substrate

*Chandreswar Mahata[a], Il-Kwon Oh[a], Chang Mo Yoon[a], Chang Wan Lee[a], Jungmok Seo[a], Hassan Algadi[a], Mi-Hyang Sheen[b], Young-Woon Kim[b], Hyungjun Kim[a], Taeyoon Lee[a]**

[a]Nanobio Device Laboratory, School of Electrical and Electronic Engineering, Yonsei University, 134 Shinchon-Dong, Seodaemun-Gu, Seoul 120-749, Republic of Korea

[b]Department of Materials Science and Engineering, Seoul National University, Gwanak-Gu, Seoul 151-744, Korea

* Corresponding author:

Tel: +82-2-2123-5767

Fax: +82-2-313-2879

e-mail address: taeyoon.lee@yonsei.ac.kr

CET and k_{eff} calculation

Capacitance equivalent thickness (CET) extracted

$$CET = \varepsilon_0 k_{SiO_2} / C_{ox} \quad (1)$$
$$= 8.854\times10^{-12}\text{F/m}*3.9*7.85\times10^{-9}\text{m}^2/1.5\times10^{-10}\text{F}$$
$$= 1.8\times10^{-9}\text{m}$$

from the low frequency f_{100Hz}(100Hz, as it is close the oxide capacitance) C–V curve was 1.8 nm for the $Ta_{1-x}Zr_xO$ on InP. Here k_{SiO2} is relative permittivity of SiO_2, C_{ox} is accumulation capacitance per unit area, and ε_0 is the free space permittivity [1].

The equivalent $k_{Ta1-xZrxO}$ value can was calculated as,

$$k_{Ta_{1-x}Zr_xO} = k_{SiO_2} T_{ox} / CET \quad (2)$$
$$= 3.9*9.2\text{nm}/1.8\text{nm}$$
$$= 19.93$$

where T_{ox} is the total physical thickness of the dielectric layer can be attained from TEM image. From above relation we have achieved high equivalent dielectric constant value of ~20 of $Ta_{1-x}Zr_xO$ nanolaminated dielectric.

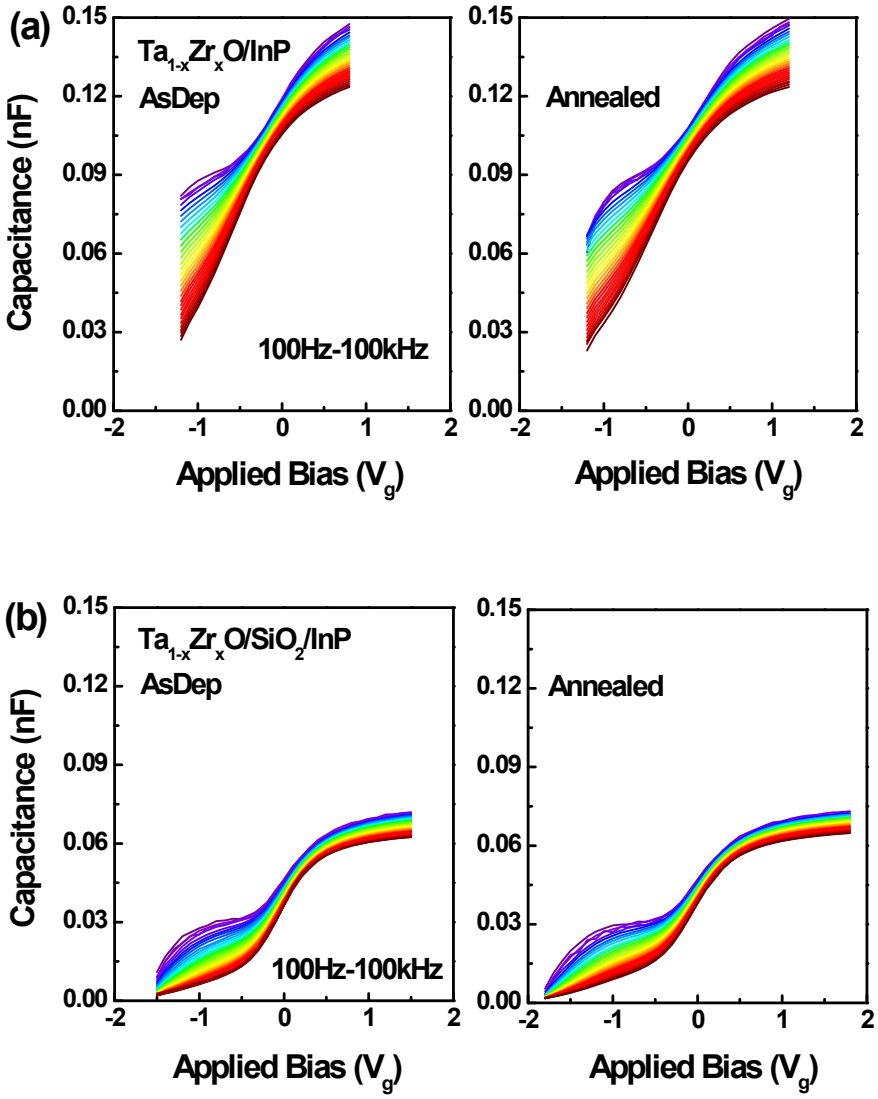

Figure S1. Capacitance-voltage characteristics of (a) TaN/$Ta_{1-x}Zr_xO$/n-InP MOS capacitor, and (b) TaN/$Ta_{1-x}Zr_xO$/ SiO_2/n-InP MOS capacitor under as-deposited and annealed (PDA) conditions.

The conductance method has been widely used to calculate accurately reliable D_{it} estimated around midgap, as the trap response is strongly temperature dependent. Another criteria for accurate measures of the D_{it} can be obtained for high-k/III-V interfaces provided that the D_{it} is sufficiently low, for $C_{ox} > qD_{it}$, where C_{ox} is the accumulation capacitance density of the high-k oxide and q the electronic charge[2]. The movement of conductance peaks in the contour maps given in the manuscript is a sign of the conduction band bending efficiency as a

function of applied gate bias [3]. Interface trap density (D_{it}) as a function of trap energy lavel (ΔE) can be calculated with the help of following equations:

$$D_{it} \approx 2.5 \frac{(G_p / \omega)_{\max}}{Aq} \tag{3}$$

$$f = \frac{1}{2\pi\tau} = \frac{\upsilon_{th}\sigma N}{2\pi} \exp\left[\frac{-\Delta E}{k_B T}\right] \tag{4}$$

where q is the electronic charge, A is the area of the capacitor, $(G_p/\omega)_{max}$ is maximum peak of conductance map, f is the applied frequency, where τ is the characteristic trapping time, σ is the trap capture cross section, υ_{th} is the carrier thermal velocity, and N is the density of state in the conduction band. The conductance peak shift indicates that the n-InP surface potential responds efficiently to the gate bias when the Fermi level is located between conduction band edge and midgap.

The D_{it} values in upper half bandgap were extracted from the n-type TaN/$Ta_{1-x}Z_xO$/SiO_2/InP devices. The D_{it} value near the conduction band was at 0.27 eV was $4\times10^{12}cm^{-2}eV^{-1}$. In case of TaN/$Ta_{1-x}Z_xO$/InP interface trap density calculation results show that $qD_{it} > C_{ox}$. In this case this conductance method becomes not sensitive to extract D_{it}, and the calculated values could be overestimated by an order of magnitude [3]. So for without SiO_2 passivation sample we could not calculate the D_{it} effectively. We also compared the D_{it} characteristics with other published recent data and has been described in Figure S2(b).

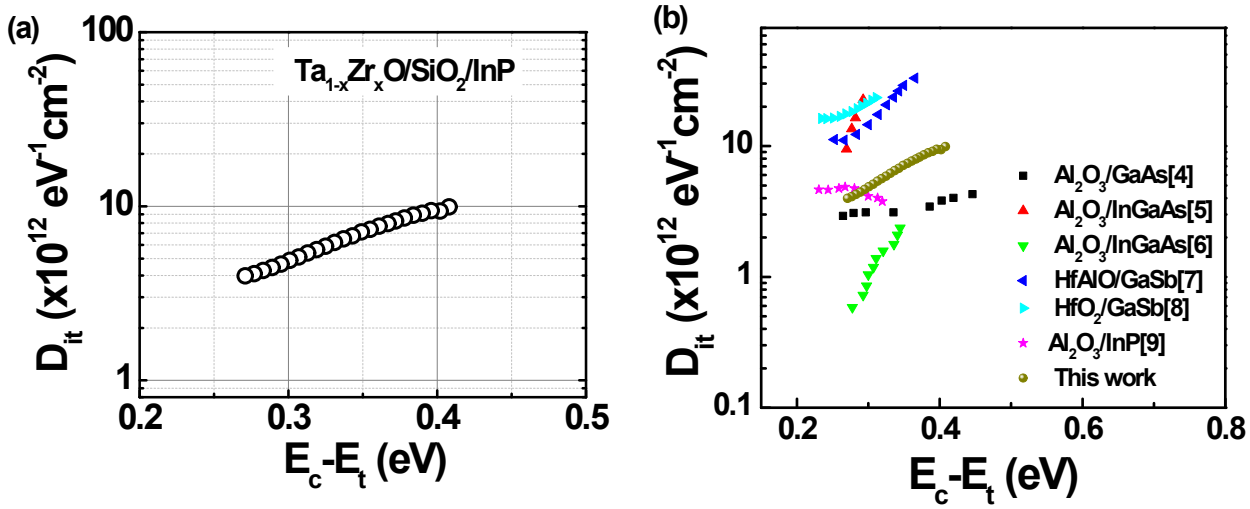

Figure S2. Interface trap distribution of TaN/$Ta_{1-x}Zr_xO$/SiO_2/n-InP MOS capacitor in the InP band gap obtained from the conductance measurement. (b) Comparison of D_{it} with different published data recently.

We have calculated the apparent doping profile from high frequency capacitance-voltage (C_{hf}–V_g) characteristics. The depletion depth (X_{dHF}) and apparent doping (N_{appHF}) as a function of applied gate potential (V_g) are expressed as follows [10]:

$$X_{dHF}(V_g) = \varepsilon_{InP}\left(\frac{1}{C_{HF}(V_g)} - \frac{1}{C_{OX}}\right) \tag{5}$$

$$\frac{1}{N_{appHF}(V_g)} = \left(\frac{q\varepsilon_{InP}}{2}\right)\left(\frac{\delta(1/C_{HF}^2(V_g)}{\delta V_g}\right) \tag{6}$$

where ε_{InP} is the InP permittivity, C_{ox} is the gate oxide capacitance/area, q is the electronic charge.

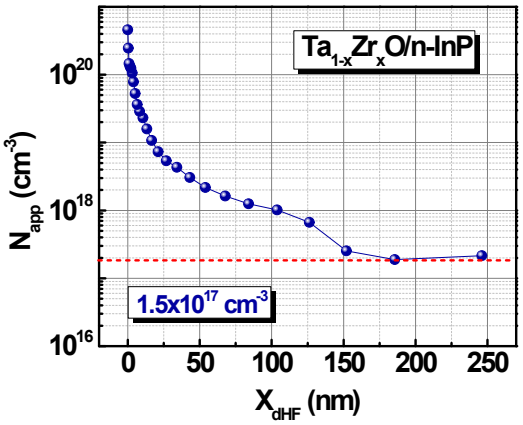

Figure S3. Apparent doping profiles for the n-InP layer from MOS capacitor high frequency C–V characteristics.

Our calculated apparent substrate doping was calculated to be approximately 1.5×10^{17} cm^{-3}, which very close to the value supplied from the manufacturing semiconductor company.

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