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Supplementary document: Effect of device geometry and crystal orientation on the stress-dependent offset voltage of 3C-SiC(100) four terminal devices

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Growth and characterization of 3C-SiC

P-type 3C-SiC was grown to a thickness of 300 nm by Low pressure chemical vapor deposition technique [1,2] in which SiH_4 and C_2H_2 were employed as the precursors. The *in situ* doping of the 3C-SiC film was performed using Trimethyaluminium (TMAl) precursor as a source of Al p-type dopant. The alternating supply epitaxy (ASE) approach was used to achieve single crystalline SiC thin film deposition. With the supply of SiH_4, Si atoms are adsorbed on the SiC surface and arrange themselves in a self-assembled pattern. When TMAl is introduced, Al–CH_3 bonds break below 528°C, and Al atoms are then adsorbed on the Si-terminated surface. Finally, the supply of C_2H_2 enables the adsorbed Si and Al atoms to be converted into SiC layers. The diffusion of Al to the Si substrate was prevented by an undoped SiC buffer layer over Si. The quality of the SiC film was investigated by X-ray diffraction analysis, selected area electron diffraction (SAED) and transmission electron microscopy. The X-ray diffraction pattern shows that the 3C-SiC is epitaxially grown on p-type Si(100). The FWHM values of the 3C-SiC(200) is 0.26° which indicates good crystalline quality of the grown film. The selected area electron diffraction (SAED) confirms that the grown 3C-SiC is single crystalline. In order to check the boundaries and stacking faults the transmission electron microscopy (TEM)

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of the film was carried out. It is evident from the transmission electron microscopy (TEM) image that there are no boundaries in the single crystalline 3C-SiC and the only defects are staking faults. [2]

Fabrication of Devices

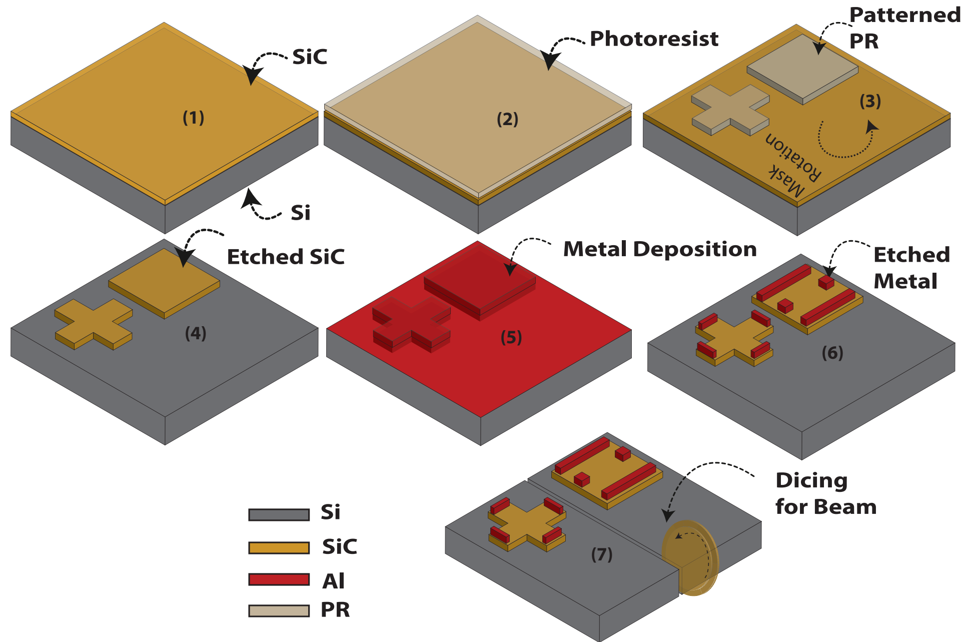

Figure 1: Fabrication process of four terminal devices, the devices with different orientations were fabricated by rotating the mask during photolithography process with respect to the reference axis of the wafer

Three different geometries of the devices at three different orientations were fabricated using standard photolithography and dry etching processes. In dry HCl and O_2 were employed as the active gases. The orientation of the devices within the (100) crystal plane was varied by rotating the mask during photolithography process. Aluminium was used for depositing Ohmic contacts to the device. After fabrication of the device, wafer was diced into strips of dimensions 60 mm × 9 mm × 0.625 mm to apply strain by the bending beam method. Figure 1 explains all the steps in fabrication of the devices.

Leakage current

As the devices are fabricated by growing 3C-SiC on Si substrate, it is important to investigate the leakage of the current through the SiC/Si heterojunction to the Si substrate. In SiC/Si heterojunction, a large valence band off-set (1.7 eV) between SiC and Si impedes the flow of holes through the junction. When SiC is positively biased with respect to the Si, depletion region across the junction increases and hence the leakage current is small. The I-V characteristics of SiC/Si heterojunction were carried out using HP 4145B analyzer

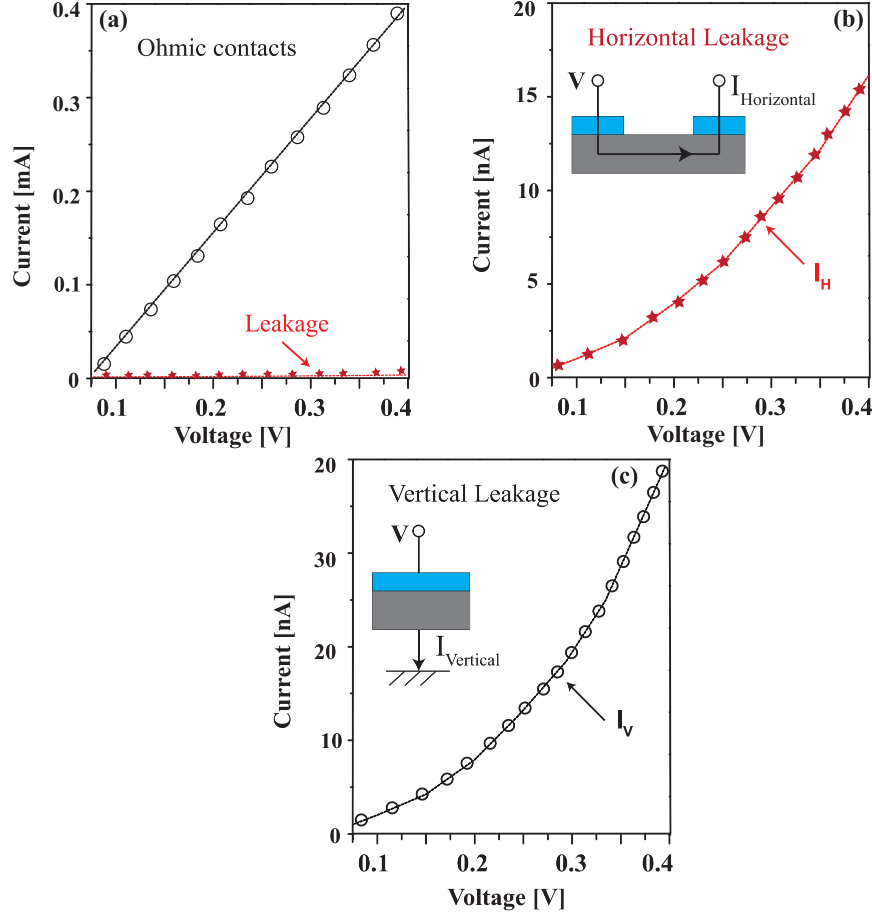

Figure 2: (a) Ohmic behavior of the contacts and leakage through SiC/Si junction; (b) Horizontal leakage through the SiC/Si junction; (c) Vertical leakage through SiC/Si junction.

by sweeping a voltage of SiC from 0 to 0.4 V with respect to Si.Both the vertical current leakage (from SiC to Si substrate), and the horizontal current leakage (from one SiC electrode to the Si film underneath and returning to another SiC electrode) were investigated.

Figure 2 (a) shows the ohmic behavior of the contacts and the leakage current through the junction, indicating that both contacts are perfectly ohmic and leakage current is negligible. Both the vertical and horizontal current leakages through the junctions at positive bias voltages are relatively small. At a voltage applied to the device of 50 mV, the total current leakage in these two cases were measured to be approximately 5 nA, which is 0.1% of the supplied current. Therefore, we consider that the current leakage through the junction does not contribute to the measurements.

Application of stress

To investigate the effect of stress on the fabricated devices the strain was induced to the devices by bending beam (bi-layered) model in which one end of the Si beam with 3C-SiC devices was fixed, while the other end

was bent by attaching different loads (Fig. 3). The lateral strain induced in 3C-SiC is:[3]

$$\varepsilon_{SiC}(x) = -\frac{F}{wD_1}(L_1 + L_2 - x)t_n \tag{1}$$

where F is the applied force, t_n is the distance from the SiC layer to the neutral axis of the Si beam and the dimensions w, L_1 and L_2 are as mentioned in fig 3. D_1 is called the bending moment and is deduced from:[4]

$$D_1 = \frac{E_1^2 t_1^4 + E_2^2 t_2^4 + 2E_1 E_2 t_1 t_2 (2t_1^2 + 2t_2^2 + 3t_1 t_2)}{12(E_1 t_1 + E_2 t_2)} \tag{2}$$

where E_1 is the Young's modulus of SiC (330 GPa),[5] E_2 is the Young's modulus of Si (130 GPa in [100]

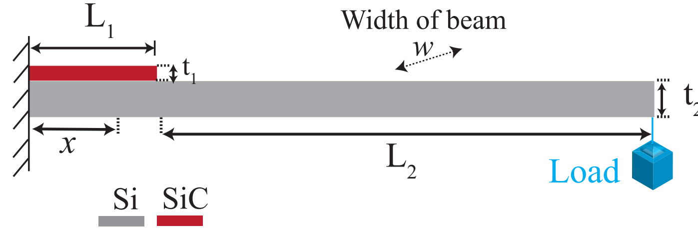

Figure 3: Schematic diagram of the bending experiment for measuring the strain in by bi-layer model.

and 169 GPa in [110] orientation), t_1 is thickness of SiC thin film and t_2 is the thickness of Si beam. The strain calculated from Eq. 1 is approximately equal to the strain induced at the surface of the Si beam as the thickness of the SiC thin film is only 0.05% of the thickness of Si.[6] Finally, the stress applied to the SiC layer (σ_{SiC} was then calculated using Hooks law: $\sigma_{SiC} = \varepsilon E_{SiC}$, where $E_{SiC} = 330$ GPa is the Youngs modulus of 3C-SiC.[5] The applied stress calculated from this method varied from -264 MPa to 264 MPa.

References

(1) Wang, L.; Dimitrijev, S.; Han, J.; Tanner, P.; Lacopi, A.; Hold, L. Demonstration of p-type 3C -SiC grown on 150 mm Si(1 0 0) substrates by atomic-layer epitaxy at 1000 C. *J. Cryst. Growth* **2011**, *329*, 67–70.

(2) Phan, H. P.; Dao, D. V.; Tanner, P.; Nguyen, N. T.; Wang, L.; Zhu, Y.; Dimitrijev, S. Fundamental piezoresistive coefficients of p-type single crystalline 3C–SiC. *Appl. Phys. Lett.* **2014**, *104*, 111905.

(3) Gao, X.; Shih, W.-H.; Shih, W. Y. Induced voltage of piezoelectric unimorph cantilevers of different nonpiezoelectric/piezoelectric length ratios. *Smart Mater. and Struct.* **2009**, *18*, 125018.

(4) Li, X.; Shih, W. Y.; Aksay, I. A.; Shih, W.-H. Electromechanical behavior of PZT-Brass unimorphs. *J. Am. Ceram. Soc* **1999**, *82*, 1733–1740.

(5) Iacopi, F.; Walker, G.; Wang, L.; Malesys, L.; Ma, S.; Cunning, B. V.; Iacopi, A. Orientation-dependent stress relaxation in hetero-epitaxial 3C-SiC films. *Appl. Phys. Lett.* **2013**, *102*, 011908.

(6) Phan, H. P.; Tanner, P.; Dao, D. V.; Nguyen, N. T.; Wang, L.; Zhu, Y.; Dimitrijev, S. Piezoresistive effect of p-type single crystalline 3C–SiC thin film. *IEEE Electron Device Lett.* **2014**, *35*, 399.