SUPPORTING INFORMATION

The effect of Tuning the Microstructure of TIPS-Tetraazapentacene on the Performance of Solution Processed Thin Film Transistors

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Content:

1. Synthesis:

TIPS-TAP was synthesised following the procedure described by *Miao et al.*.[1] Column chromatography was performed as first purification step (silica gel, PE/CH_2Cl_2) and gave **TIPS-TAP** (R_f = 0.10, PE/CH_2Cl_2 = 3:1) as dark green crystalline material (yield 97%). The compound was further purified by several recrystallization processes from hexane and ethanol solutions.

After one day in solution traces of the reduced species of **TIPS-TAP** can be detected in NMR-spectroscopy. Therefore, all solutions of **TIPS-TAP** for our studies were always prepared freshly.

Sublimation/ Evaporation at low pressure (10^{-5} mbar) failed as our sublimated material exhibits traces of an additional side product (R_f (side product) = 0.79, R_f (TIPS-TAP) = 0.64, PE/CH_2Cl_2 = 10:1) and IR spectra show additional vibrations for the sublimated material between 2350 cm^{-1} and 2420 cm^{-1}.

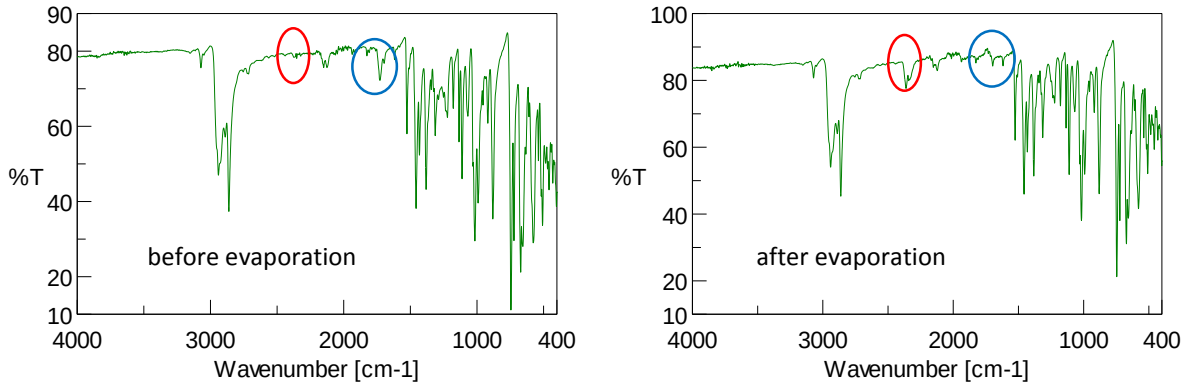

Figure S-1. IR-spectra of TIPS-TAP before and after sublimation.

2. Thin film & device preparation:

Polyimide coated glass:

All films on glass/polyimide were prepared on pre-cut 1737F glass substrates (PGO, Iserlohn, Germany) following the reported procedure.[2] A ca. 30 nm thick Polyimide layer (diluted PI-2525, Hitachi Chemical DuPont MicroSystems GmbH, Neu-Isenburg, Germany) was used to support a good crystallisation and homogenous film formation. The polyimide film was cross linked at 300 °C for 3h.

BCB coated Si/SiO_2 samples:

P-doped (boron) silicon wafers (001) with a thermally grown 250nm silicon dioxide were purchased from ABC GmbH (Brunnthal, Germany) and manually cut into appropriate size. The samples were then rinsed in acetone and isopropyl-alcohol in an ultrasonic bath for 5 minutes and dried with compressed air. After oxygen plasma treatment for 10 min a ca. 50 nm thick BCB (benzocyclobutene) layer was spin coated (CYCLOTENE 3035-22, kindly provided by M.Töpper, Fraunhofer IZM, Berlin, Germany) and cross-linked under nitrogen atmosphere at 290 °C for 60 s.[3]

TIPS-TAP film preparation:

TIPS-TAP films were spin coated at 1500 rpm for 30 s from freshly prepared solutions of toluene, chlorobenzene, *m*-xylene, mesitylene with a concentration of 10 mg/ml and 20 mg/ml and annealed at 80 °C for 15min on either polyimide coated glass substrates or BCB coated Si/SiO_2-wafers. The average film thicknesses were between 25-50 nm. Films cast from toluene and tetralin had thicknesses of 40-50 nm, while films from chlorobenzene and xylene had thicknesses ranging from 25 to 35 nm. Films deposited from Tetralin were spin coated at 900 rpm for 30 s and dried at 80 °C for 15 min. Films for AFM, UV-VIS and XRD were prepared on polyimide coated glass substrates prepared in an identical fashion to those prepared for device fabrication.

FET fabrication:

Bottom-contact top-gate (BC/TG) transistors were fabricated on polyimide coated glass substrates. Gold source and drain electrodes (20 nm thick, W = 1000 µm, L = 5, 10, 20 and 50 µm) were patterned by double layer resist photolithography. After lift-off in *N*-Methyl-*2*-pyrrolidon, the substrates were transferred into a N_2 glovebox for all subsequent processing steps. The deposition of the active layer followed the procedure above. A ca. 650 nm thick layer (C = 4.90 nF/cm²) of PMMA (Polymer Source, Dorval, Québec, Canada) was spin coated as dielectric layer from acetonitrile and dried at 90 °C for 30 min. Finally, a 20 nm thick silver gate electrode was evaporated through a shadow-mask. Layer thicknesses were determined by a stylus profiler (DektakXT, Bruker).

The active layer for Bottom-gate top-contact transistors (BG/TC) was deposited as described above. The device were finished by an evaporation of gold-contacts through a shadow mask (W = 1500 µm, L = 130, 180, 230 µm).

Zone Casting:

A home-built Zone-Casting setup was used to ensure aligned crystallisation of the **TIPS-TAP** semiconductor. The substrates were placed on a heated aluminium block and moved using stepper motors at a constant speed (150 µm/s) below a heated nozzle that slowly supplied the organic solution (mesitylene, 3 mg/ml). The nozzle was kept at a temperature 20 °C lower than the substrates

temperature. A substrate temperature of 120 °C resulted well aligned and orientated crystals of **TIPS-TAP**. Lower temperatures resulted non-aligned and small crystallites while higher temperatures caused cracks in the ribbons and non-uniformity in thickness.

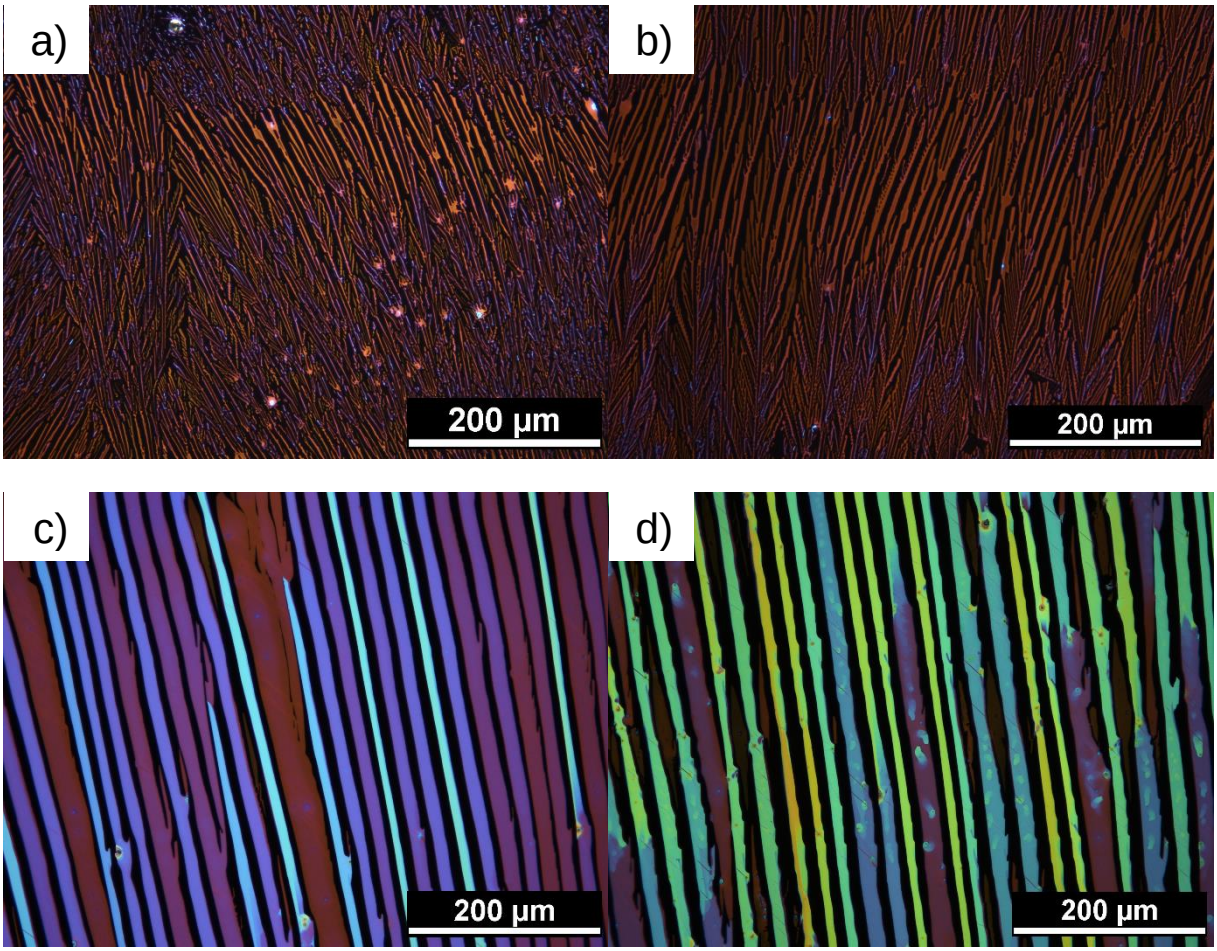

Figure S-2. Optical microscope images of zone-cast films of TIPS-TAP under crossed polarisers at various substrate temperatures on BCB a) 90 °C b) 100 °C, c) 120 °C and d) 130°C.

Films for FET fabrication were cast at 120 °C and a speed of 150 µm/s for BG/TC on BCB coated Si/SiO_2 wafers and for BC/TG FETs on polyimide coated glass with structured gold electrodes. The devices were finished following the remaining steps for each transistor architecture.

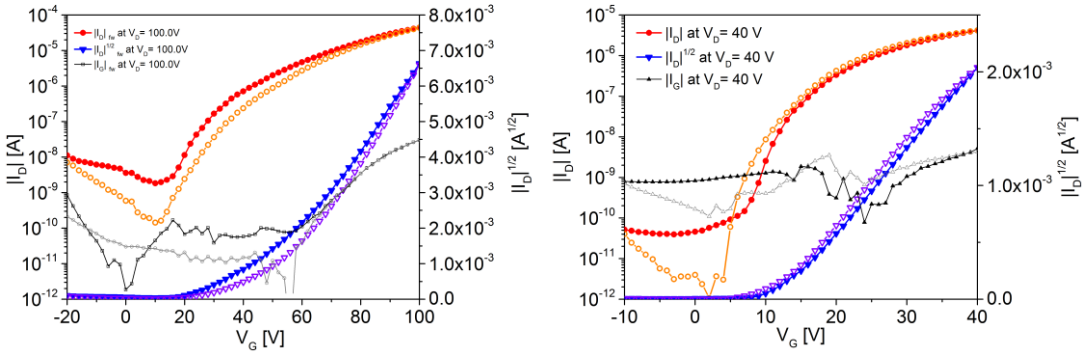

Figure S-3. Transfer characteristics for zone-cast **TIPS-TAP** OFETs. Left: in BC/TG architecture on polyimide (L=20 µm, W=1000 µm); right: in BG/TC architecture on BCB (L=250 µm, W=1500 µm).

3. General Methods:

Thin films of TIPS-TAP were spin coated on Au (50nm)/Si substrates for Ultra-Violet photoemission spectroscopy (UPS). The samples were then transferred into the ultrahigh vacuum (UHV) chamber (ESCALAB 250Xi) for UPS measurements. The measurements were performed using a double-differentially pumped He gas (hν = 21.22 eV) with a pass energy of 2 eV. Absorption spectra were recorded on a Jasco UV-VIS V-670. Cross-polarised optical microscopy images were taken using a Nikon Eclipse LV100POL microscope. Atomic Force Microscopy (AFM) was performed in tapping mode using a Digital Instruments Nanoscope IIIa microscope under ambient conditions. AFM images were processed (polynomial background removal) using the Gwyddion 2.33 software. Electrical characterisation of all devices was performed under nitrogen with an Agilent 4155B Semiconductor Parameter Analyser or a Keithley 4200 SCS. Electron mobility values μ_e (cm^2/Vs) were extracted from a linear fit of the transfer characteristics in the saturation regime using the following equation:

$$\mu = \left(\frac{\partial\,(I_D)^{1/2}}{\partial V_G}\right)^2 \frac{2L}{WC}$$

where I_D is the source-drain current [A], VG the gate voltage [V], W and L are the channel width and length [m], respectively, and C [F/m^2] is the dielectric layer capacitance per area unit. The intercept of the linear fit with the gate voltage axis gave V_{th}. The characteristic device parameters were averaged from several batches of similarly performing devices with varying channel lengths. The devices were measured with a hold-time of 0.5 s and a delay time of 0.25 s. The FETs measured from off to on

including a double sweep (forward-backward). Devices with defects (e.g. high gate leakage or shorts) were not used for analysis.

X-ray diffraction experiments were performed in symmetrical Bragg-Brentano geometry using a Seifert FPM URD6 diffractometer equipped with a sealed X-ray tube with Cu anode operating at 40 kV and 30 mA. Primary beam divergence was limited to 0.018 rad by a vertical divergence slit. The secondary beam was filtered using a curved graphite monochromator, thus the detectable Bragg reflections were recorded with the $K\alpha_{1,2}$ doublet from the Cu anode (wavelength 1.54056 Å/1.54437 Å). Photons were counted with a scintillation detector. Diffraction patterns were recorded from $2\theta = 3°…40°$ in steps of 0.02°. Reflection positions (see **Table S-1**) were determined by fitting pseudo-Voigt function doublets, considering the two-wavelength character of the employed radiation, to the particular peaks.

4. XRD diffraction data:

Table S-1. Summarised XRD data for TIPS-TAP films spin-coated on polyimide coated glass substrates: Peak positions and d spacings of the (001) calculated via Braggs law and $d_{(001)} = l \times d_{(00l)}$.

(*hkl*)	toluene		chlorobenzene		xylene		mesitylene		tetralin	
	2θ [°]	$d_{(001)}$ [Å]	2θ [°]	$d_{(001)}$ [Å]	2θ [°]	$d_{(001)}$ [Å]	2θ [°]	$d_{(001)}$ [Å]	2θ [°]	$d_{(001)}$ [Å]
(001)	5.35	16.50	5.36	16.47	5.32	16.61	5.33	16.58	5.36	16.47
(002)	10.72	16.49	10.74	16.46	10.71	16.51	10.74	16.46	10.72	16.49
(003)	16.10	16.51	16.12	16.48	16.10	16.50	16.10	16.50	16.10	16.50
(005)	27.01	16.49	27.01	16.49	26.99	16.51	27.03	16.48	27.06	16.46
		avg. **16.50**		avg. **16.48**		avg. **16.53**		avg. **16.51**		avg. **16.48**

5. Film Morphology:

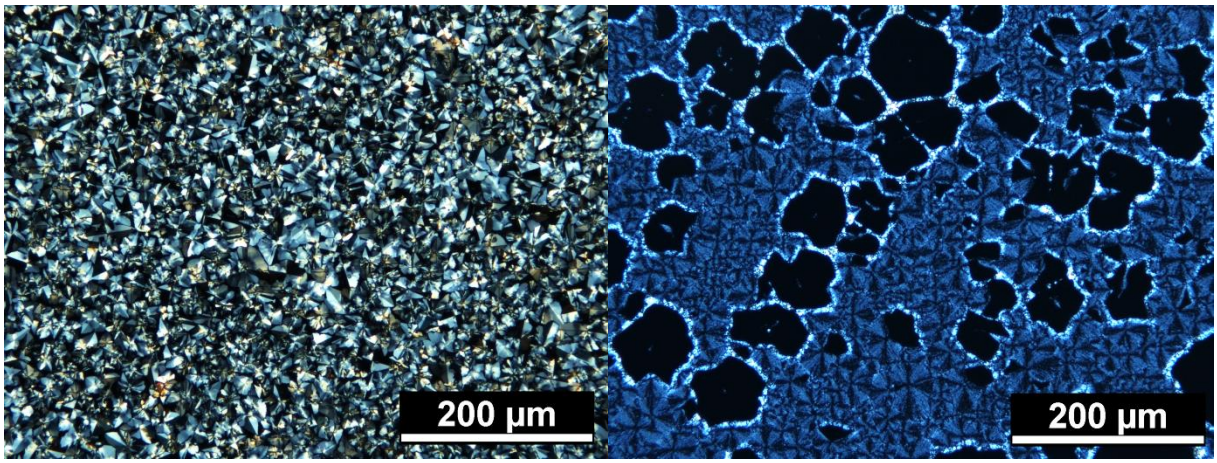

Figure S-4. Cross polarised optical images of film from TIPS-TAP on bare glass. **Left image:** very rough film deposited from toluene solution (20mg/ml); **Right image:** non-continuous film of TIPS-TAP due to partial dewetting, spin coated from *m*-xylene (10 mg/ml).

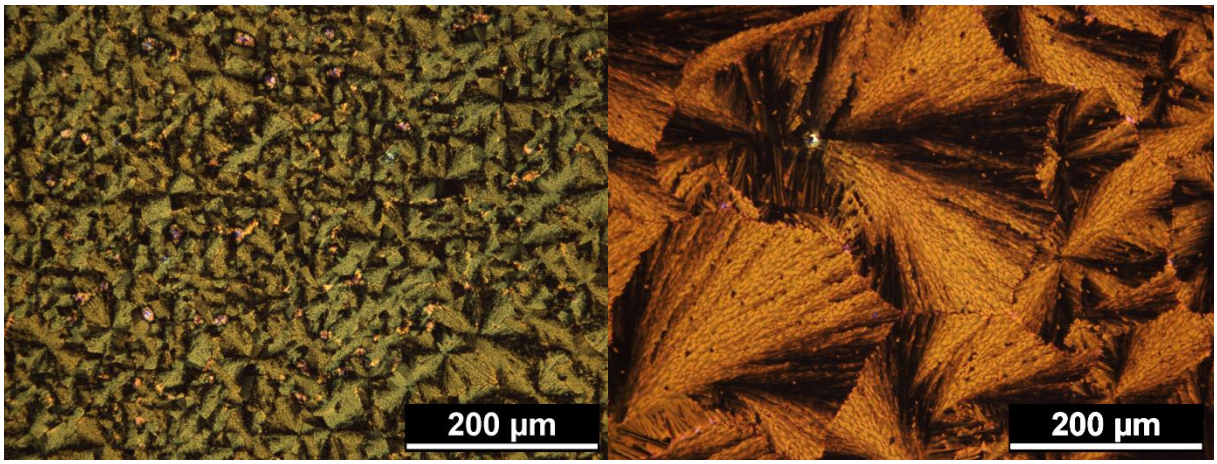

Figure S-5. Cross polarised optical micrographs of film from TIPS-TAP on BCB/SiO_2/Si. **Left image:** film deposited from mesitylene solution (10 mg/ml); **Right image:** polycrystalline film of TIPS-TAP spin coated from tetralin (10 mg/ml).

Table S-2. Summarised transistor parameters for BG/TC OFETs of TIPS-TAP fabricated on BCB.

Solvent	**Boiling point** [°C]	**best μ_e** [cm^2/Vs]	**average μ_e** [cm^2/Vs]	**average threshold voltage** [V]	**on/off ratio** [ ]
Mesitylene	165	0.07	$(5.8\pm0.3)\cdot10^{-2}$	9.5±0.3	10^3-10^4

6. Bias Stress:

For Bias-Stressing BG/TC transistors on BCB were used and fabricated following the procedure above. All single FETs on the substrate were connected through pins and kept in a nitrogen filled box. The bias stress experiment was performed using two Keithley 2450 SMUs to measure I_{drain} and I_{gate} while Source was put on common. The FETs were biased with $V_D = V_G = 40$ V for 20 min directly followed by a Transfer measurement in the saturation regime ($V_D = 50$ V) (from off-on). The stressed FET was then given a resting time of 40 min while other FETs on the same substrate were stressed and probed. The hold and delay times were identical to the measurements reported above. Mobility and threshold voltages were obtained from a linear fit of the transfer characteristics. The relative hysteresis is calculated as the relative difference in area between forward to backward sweeps.

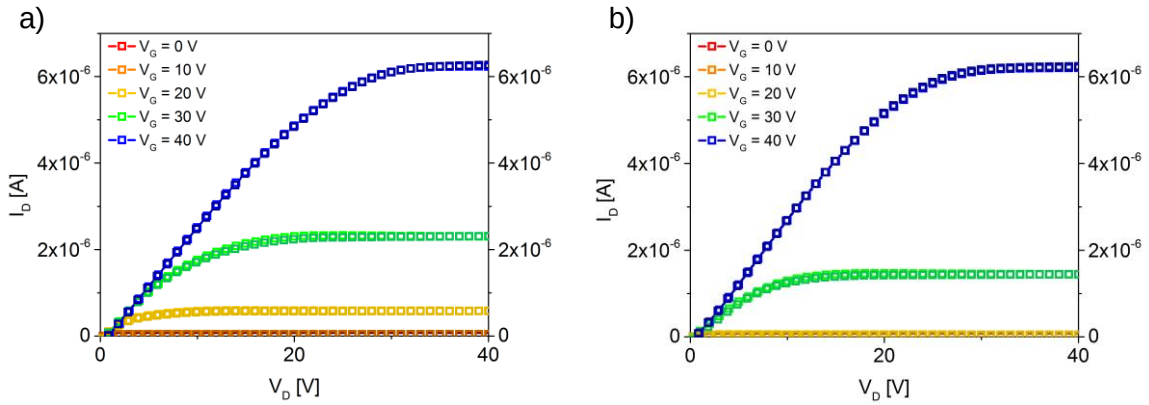

Figure S-6. Output characteristics of a stressed FET showing linear injection behaviour during the stress experiment a) prior to the first bias stress b) after 850 min in the stress experiment. In both cases almost no hysteresis is present.