Supplementary Information for multichannel detection of ionic currents through two nanopores fabricated on integrated Si₃N₄ membranes

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SI-1. Photographs of the flow cell and chip

Fig. S-1(a) shows the top and bottom of the membrane array chips. Fig. S-1(b) shows the bottom and upper parts of a flow cell.



Fig. S-1

SI-2. Capacitance measurements in the back isolation setup with a nonoxidized chip

Fig. S-2 shows two results of the capacitance measurements in the back isolation setup with a non-oxidized chip. In each case, the capacitance across the membrane, and the capacitance between two adjacent chambers with and without a KCl aqueous solution in the common chamber were measured. In the case of (1), all data was obtained at AC/DC bias = 500/0 mV. In the case of (2), AC/DC bias = 200/500 mV was used for the measurement across the membrane, and AC/DC bias = 100/500 mV was used for the measurements between two adjacent chambers. Table. S-2 shows the value of C_p and tan δ at 40 Hz in each case. In the case of (1), tan δ at 40 Hz exceeded 0.1 and the dielectric loss could not be negligible. In the case of (2), tan δ at 40 Hz decreased to some extent, less than 0.1. Consequently, the result in (2) was chosen to discuss the capacitance in this paper. At the present time, we cannot provide a clear explanation of why the dielectric loss in the case (2) was suppressed compared to the case (1).



Fig. S-2

Table. S-2

	(1)		(2)	
	Cp @ 40Hz (nF)	$\tan \delta$ @ 40 Hz	Cp @ 40Hz (nF)	$\tan \delta$ @ 40 Hz
_	17.0	0.16	20.6	0.082
_	21.3	0.20	13.3	0.057
	17.0	0.17	8.22	0.081

SI-3. lonic currents through nanopores and their noise power spectrums

Ionic currents through nanopores (Fig. 6(a)–(c)) and their noise power spectrums (Fig. 6(d)) in the front isolation set up, back isolation setup, and back isolation setup with surface-oxidized chips were shown. These results are reasonable because the noise in the ionic current decreases with the decrease in capacitance across the membrane.



Fig. S-3