Supporting Information

Ultralow Power Complementary Inverter Circuits Using Axially Doped p- and n-channel Si Nanowire Field Effect Transistors

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~~1. Transfer characteristics (I_{ds}–~~V_g) across p-n region diode

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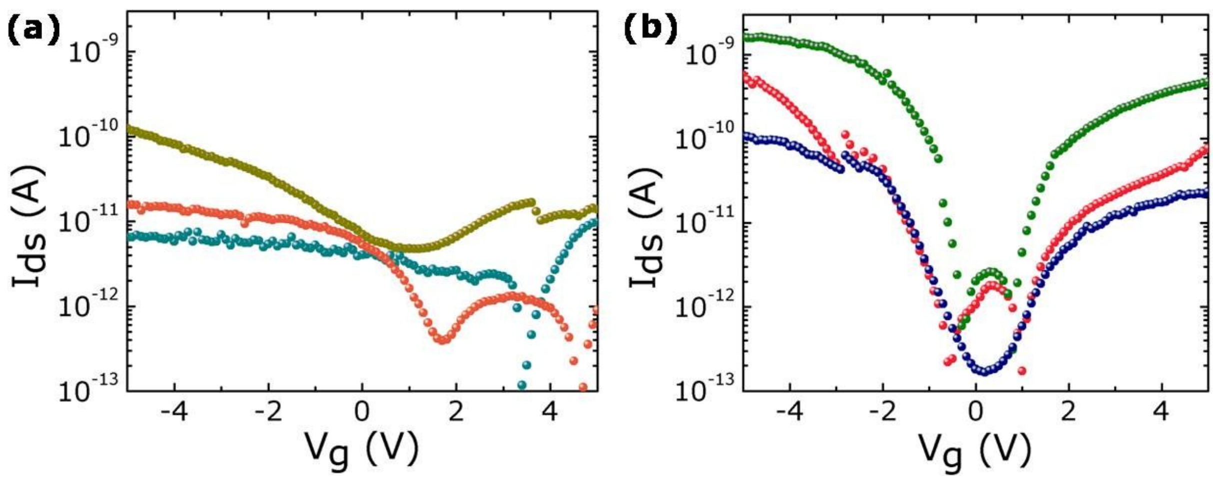

Figure S1. Transfer characteristics (I_{ds}–V_g) across p-n junction diode at (a) V_{ds} = 0.1 V and (b) V_{ds} = 1 V.

When the forward bias voltage is set above the rectifying voltage of p-n junction diode, the diode should work at ON state. Thus, the region close to the p–n junction can exhibit a clear gate effect. Therefore, the ambipolar gate effect should be observed in Si NWs p-n junction diode (Fig. S1b).[1]

On the other hand, in case where the forward bias voltage was set at 0.1 V, which is lower than the rectifying voltage of our p-n junction diodes that range from 0.15 to 0.8 V according to the doping concentrations, the diode would operate at OFF state. Thus, the low doping concentration of p- and n-type regions will be strongly affected by the gate bias as is evident from the p- and n-type Si NWFETs device characteristics (See Fig. 2f, h). In fact, if p- and n-type regions of Si NWFETs are strongly affected by the gate bias, no gate effect should be observed from the p-n junction diodes (Fig. S1a). This is because one side of junction will always be at OFF state irrespective of the polarity of the gate bias. Therefore, conductance through p-n junction is always OFF at any gate voltage.

2. Four probe measurements

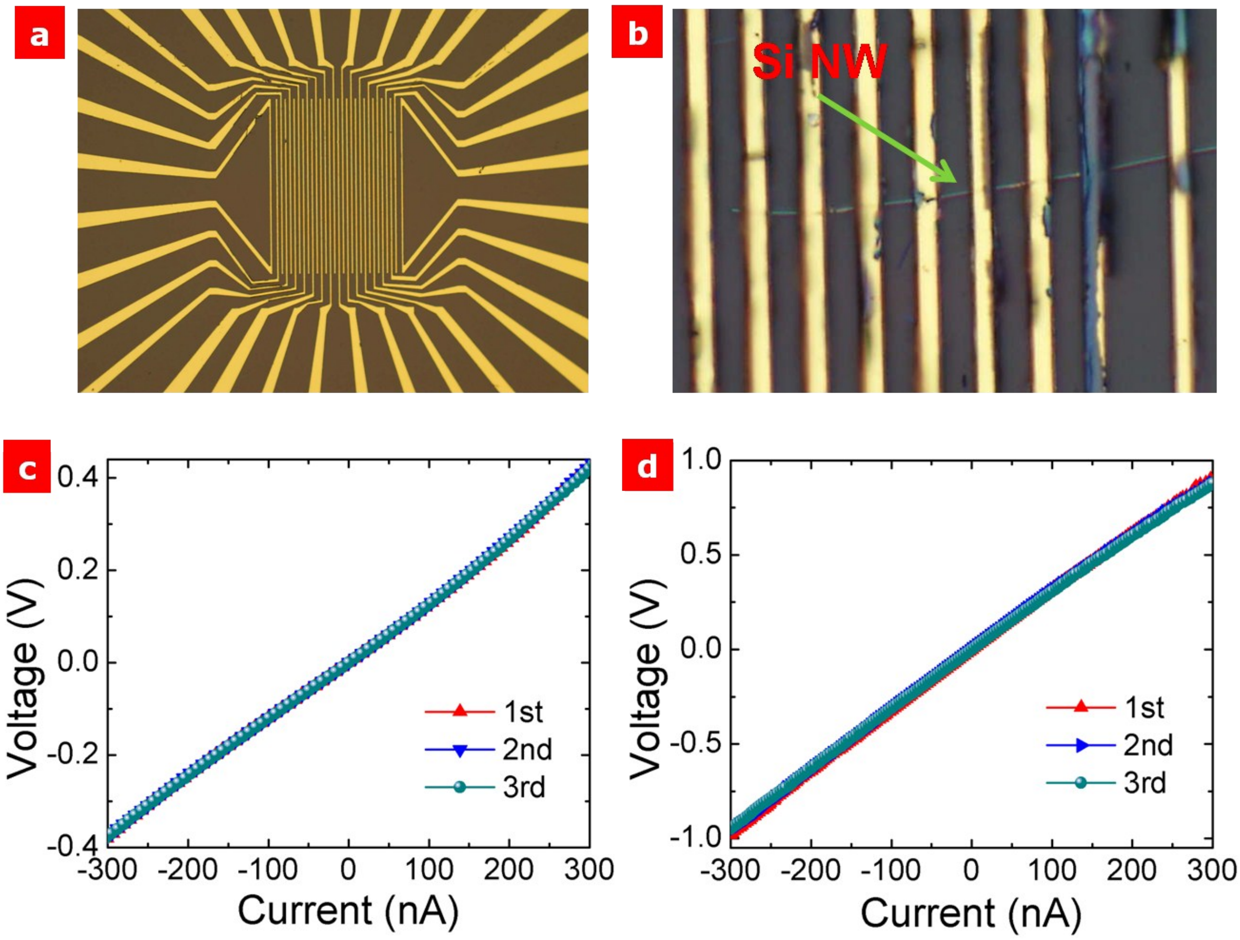

Figure S2. Optical images and electrical four-probe transport characteristics of p-n Si NW FETs. (a, b) Optical images of p-n Si NW FET devices. Four-probe voltage–current measurements of the (c) p-type region and (d) n-type region of the p-n Si NW FETs.

The p-type region of the p-n Si NW had a resistance (R) of 1.22×10^6 Ω, which was extrapolated from the linear region of the current–voltage curve obtained by the four-probe measurements shown in Fig. S1c. The resistivity, $\rho = 0.07$ Ωcm, was calculated according to $\rho = RA/L$, where $A = \pi r^2$ is the p-n Si NW cross section, L is the conducting channel length of the NW (~3.5 μm), and r is the radius of the NW (~25 nm). The resistance, $R = 3.16 \times 10^6$ Ω, and resistivity, $\rho = 0.18$ Ωcm, were calculated for the n-type regions of the p-n Si NWs from Fig. S2d.

3. Summary of electrical properties of p- and n-type regions with different gas doping concentrations

Table S1. Summary of threshold voltage, transconductance, mobility, subthreshold swing and carrier concentration for devices shown in Fig. 3a, b.

Parameters	p-type FET		n-type FET	
Doping gas concentration	**6,000:1**	**3,000:1**	**6,500:1**	**3,500:1**
Threshold Voltage (V)	**-0.5**	**-3.5**	**1.5**	**4.0**
Transconductance (nS)	**0.9**	**14.3**	**6.0**	**58.3**
Mobility (cm^2 V^{-1} s^{-1})	**3.3**	**52.9**	**22.3**	**215.7**
Subthreshold swing (mV dec^{-1})	**83.5**	**248.5**	**108.4**	**217.9**
Carrier concentration ($\times 10^{17}/cm^3$)	**1.5**	**11.0**	**4.5**	**12.0**

4. The electrical characteristics table of the p-n Si NW FETs

Table S2. Summary of the electrical transport characteristics of p-n Si NW FET devices.

	p-type FET	**n-type FET**
Resistance (×10^6 Ω)	**1.22**	**3.16**
Resistivity (Ωcm)	**0.07**	**0.18**
Transconductance (nS)	**142.4**	**108.2**
Mobility (cm^2/V.s)	**52.6**	**39.9**
Carrier concentration (×10^{17} e/cm^3)	**7.5**	**6.0**
Subthreshold swing (mV/dec)	**178**	**182**
Threshold voltage (V)	**2.5**	**-2.0**

5. Mobility comparison

Table S3. Mobility comparison between the Si NW FETs in this study and other FETs made from single p-type and n-type Si NWs reported elsewhere.

References	p-type	n-type	Ref.
	Mobility ($cm^2\ V^{-1}\ s^{-1}$)	Mobility ($cm^2\ V^{-1}\ s^{-1}$)	
Z. Jiang *et al.*	-	14	1
T. W. Koo *et al.*	25	50	2
T.-t. Ho *et al.*	28 ± 2.6	28 ± 2.6	3
K. D. Buddharaju *et al.*	112	151	4
N. H. Van *et al.*	46.2	59.3	5
This work	52.6	39.9	

References:

1. Z. Jiang, Q. Qing, P. Xie, R. Gao and C. M. Lieber, *Nano Letters*, 2012, **12**, 1711-1716.
2. T. W. Koo, D. S. Kim, J. H. Lee, Y. C. Jung, J. W. Lee, Y. S. Yu, S. W. Hwang, D. Whang, *J. Phys. Chem. C,* 2011, **115**, 23552.
3. T.-t. Ho, Y. Wang, S. Eichfeld, K.-K. Lew, B. Liu, S. E. Mohney, J. M. Redwing and T. S. Mayer, *Nano Letters*, 2008, **8**, 4359-4364.
4. K. D. Buddharaju, N. Singh, S. C. Rustagi, S. H. G. Teo, G. Q. Lo, N. Balasubramanian and D. L. Kwong, *Solid-State Electronics*, 2008, **52**, 1312-1317.
5. N. H. Van, J.-H. Lee, J. I. Sohn, S. N. Cha, D. Whang, J. M. Kim and D. J. Kang, *Nanoscale*, 2014, **6**, 5479-5483.