

# **Mechanically robust 39 GHz cut off frequency graphene field effects transistors on flexible substrate: Supporting Info.**

*Wei Wei<sup>a</sup>, Emiliano Pallecchi<sup>a</sup>, Samiul Haque<sup>b</sup>, Stefano Borini<sup>b</sup>, Vanessa Avramovic<sup>a</sup>, Alba Centeno<sup>c</sup>, Zurutuza Amaia<sup>c</sup> and Henri Happy<sup>a</sup>*

<sup>a</sup> Institute of Electronics, Microelectronics and Nanotechnology, (IEMN) CNRS UMR8520, Villeneuve d'Ascq, cedex, France.

<sup>b</sup> Nokia Technologies, 21 JJ Thomson Av., Madingley Rd, Cambridge, CB3 0FA, United Kingdom.

<sup>c</sup> Graphenea, Avenida de Tolosa, 20018 - Donostia/San Sebastián, Spain

## **Table of contents**

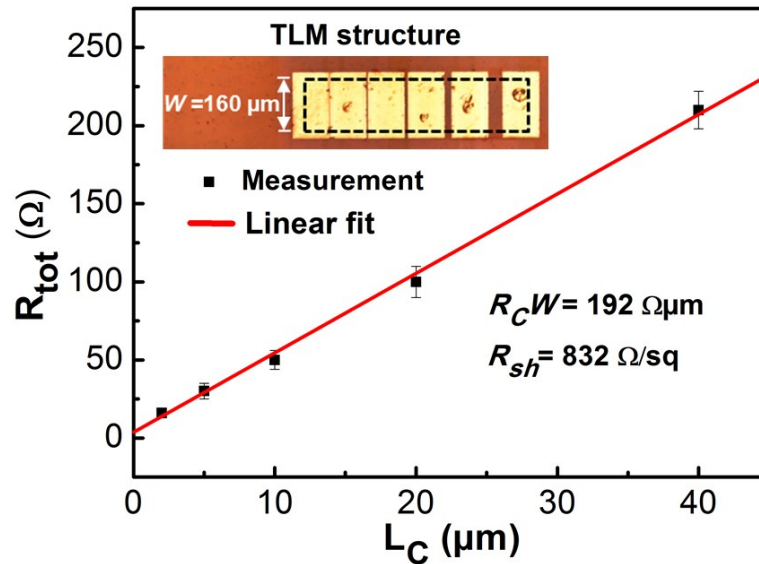
**1 – Contact Resistance**

**2 – High frequency performances versus gate length and channel width**

**3 – De-embedding example**

## S1 – Contact Resistance

To determine the contact resistance of our transistors we fabricated TLMs structures on Kapton together with our GFETs (Fig. S1 inset). The electrical contact to graphene is obtained by e-beam evaporation of 50 nm of gold (same fabrication step as for GFET). To facilitate the on-chip probe measurements, we further deposited Ni/Au (50nm/300nm in thickness) on top of Au. The width  $W$  of our TLMs is 160  $\mu\text{m}$ , while the contact spacing  $L_c$  is 2  $\mu\text{m}$ , 5  $\mu\text{m}$ , 10  $\mu\text{m}$ , 20  $\mu\text{m}$  and 40  $\mu\text{m}$ .



**Figure S1.** Two point resistance versus electrode spacing. The red line is a linear fit to the measured data. Error bars: maximum deviation from the average of three TLM structures with the identical geometry.

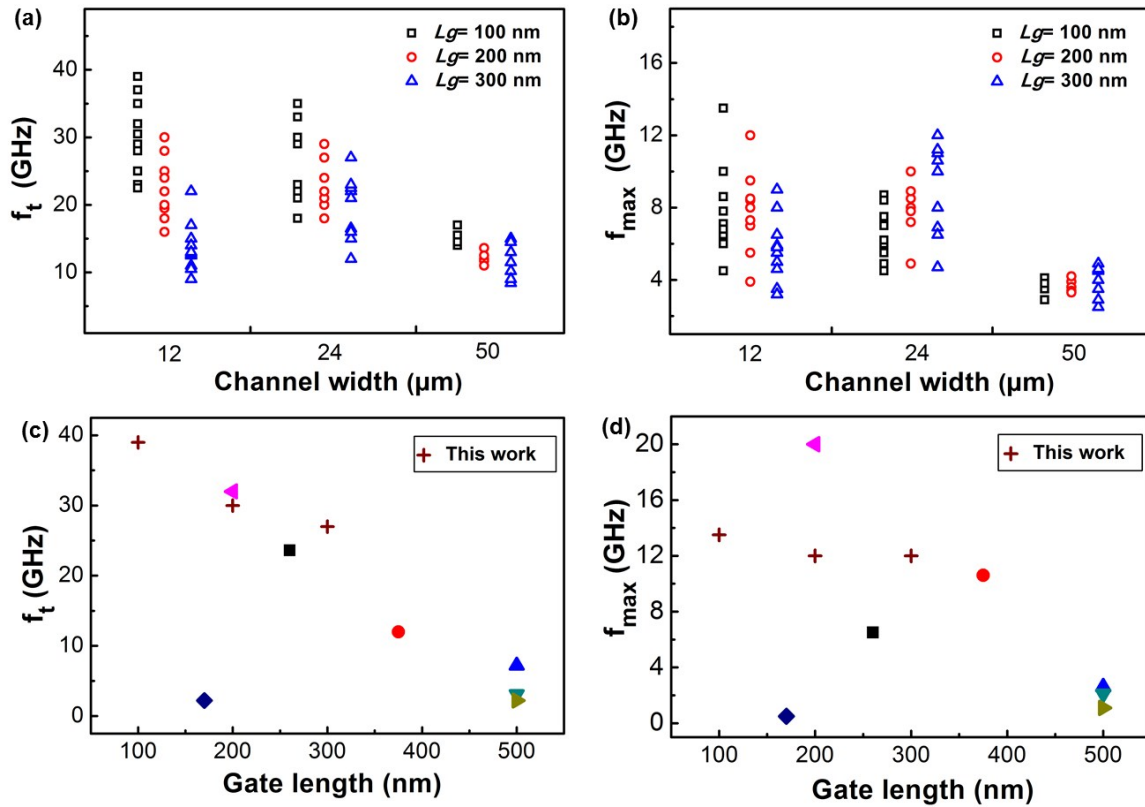
The two point resistance for the different spacing is the measured for three TLM structures. In Figure S1 we present the average resistance, the error bars represent the spreading of the measures. The contact resistance  $R_c$  is then obtained by fitting the data using the relation:

$$R_{\text{tot}}(L_c) = R_{\text{sh}}/W L_c + 2 R_c$$

The linear fit is shown in Fig S1 as a red line, it correctly reproduce the measured data. The extracted contact resistance and sheet resistance from our TLM structure are respectively 192  $\Omega\mu\text{m}$  and 832  $\Omega/\text{sq}$ . The sheet resistance is in agreement with data obtained by Hall measurement, which validates our analysis. From a mechanical point of view, we did not observe adhesion problems in TLMs nor on GFETs.

## S2 - High frequency performances versus gate length and channel width

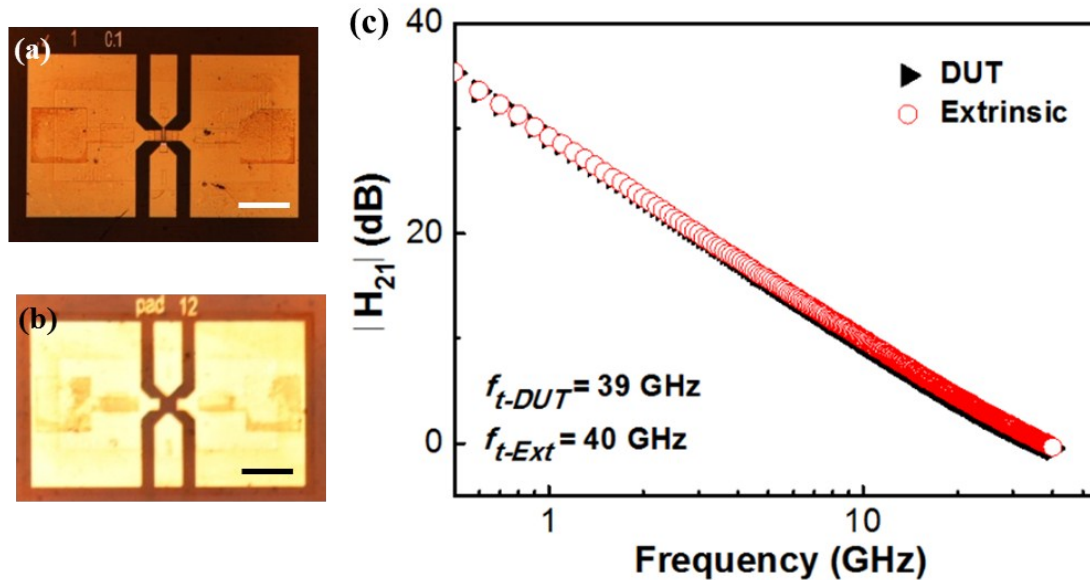
The use of large area graphene and the high yield of our process allowed us to have a large statistic of GFETs performances, which is important to assess the consistency of our work. In Figure S2 a-b we summarize the performances obtained on all our GFETs transistors ( $f_t/f_{max}$ ) for different channel width and gate lengths. These data allow us to compare (Figure S2 c-d) the best performances of our transistors with state of the art for different gate lengths. Our devices are above or close to state of the art for all the gate lengths we fabricated (100/200/300 nm), showing the reliability of our devices.



**Figure S2.** As-measured RF performance of all GFETs with different gate length and channel width, in (a) cut-off frequency  $f_t$ , in (b) maximum oscillation frequency  $f_{max}$ . Comparison of our best as-measured  $f_t$  in (c) and  $f_{max}$  in (d) with flexible GFETs reported in literatures [28-34] of main paper] according to different gate length.

### S3 - Open De-embedding example

We show in the following that the CPW has negligible effects on the RF-performances of our devices. The CPW was simulated using CST, the characteristic impedance was found to be close to 80 ohm.



**Figure S3.** (a) Optical micrograph of the GFET (at the center) with RF coplanar wave guide access. (b) Optical micrograph of the CPW de-embedding structure. The scale bar in optical micrograph is 50  $\mu\text{m}$ . (c) Measured and de-embedded current gain,  $|H_{21}|$ , of the GFET presented in the main paper.

The de-embedded procedure made in this work is similar to that presented in ref1. The de-embedding structures were fabricated on-chip together with the GFETs.

**To determine extrinsic performance:** first we measured the S-parameter matrices of both, the GFET (Figure S3-a) and the CPW de-embedding structure (Figure S3-b). This structure only contains the coplanar access, without the active part of the transistor. Then the S-matrices for GFET and CPW de-embedding structure are converted into the admittance matrices  $Y_{GFET}$  and  $Y_{CPW}$  respectively. The extrinsic admittance is then simply obtained by subtraction  $Y_{ext} = Y_{GFET} - Y_{CPW}$ . The current gain is then directly obtained from the extrinsic matrix.

The CPW de-embedding we discussed above show that the CPW does not improve significantly the performances of the flexible GFETs (Figure S3-c). A complete GFET de-embedding would also be interesting using other de-embedding structures; but it is less relevant for applications which are based on the available (extrinsic) rather than intrinsic FET performances.

#### REFERENCES :

- [1] L. Nougaret, H. Happy, G. Dambrine, V. Derycke, J. -P. Bourgoin, A. A. Green and M. C. Hersam, 80 GHz field-effect transistors produced using high purity semiconducting single-walled carbon nanotubes, Appl. Phys. Lett. 94, 243505 (2009)