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Supplementary Materials

Super Nonlinear RRAM with Ultra-low Power for 3D Vertical Nano-Crossbar Array

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S1. schematic diagram of the typical 2D crossbar array

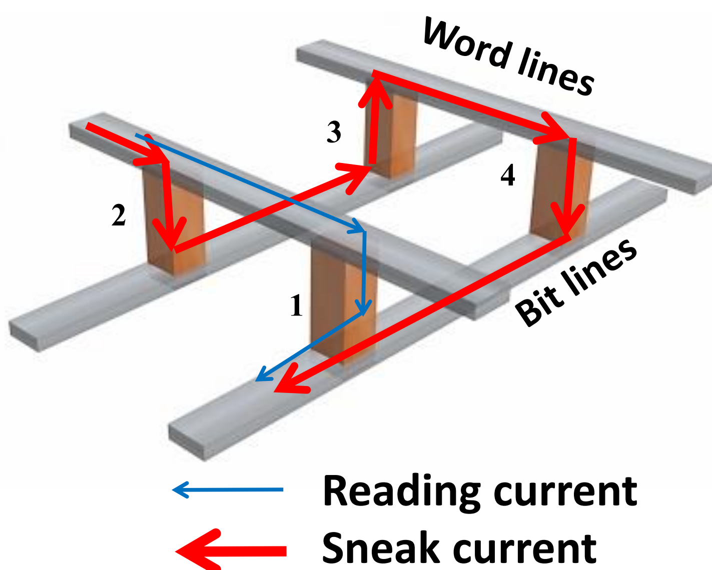

Fig. S1 A schematic diagram of the typical crossbar array showing the read disturbance problem by the presence of sneak current: read current (thin blue line), sneak current (thick red line). The sneak current through the on-state neighboring memory cells (2, 3 and 4) disturbs the reading out of the off-state cell 1. In the worst case scenario, all the neighboring memory cells are in on-state, making the problem even more serious.

S2. Schematic of stacked crossbar array and V-RRAM.

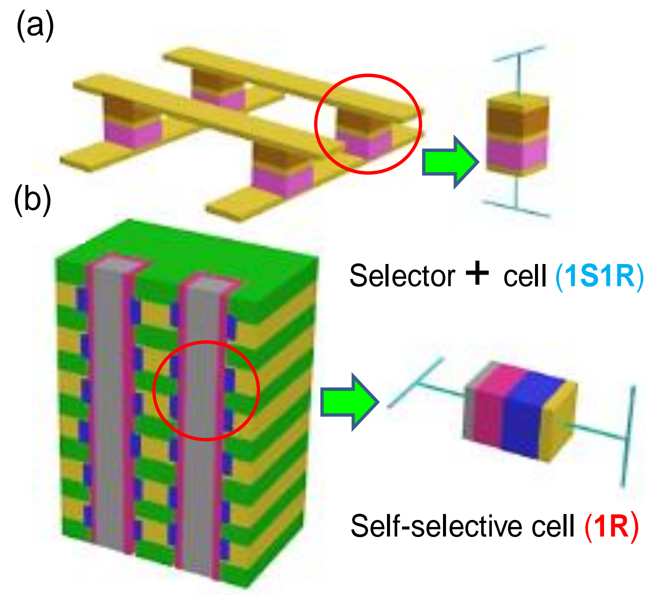

Fig. S2. The schematic of (a) planar crossbar array and (b) V-RRAM. To prevent the leakage current flowing through the unselected cells, the LRS of the memory cell should be with high nonlinearity, which could be achieved either by introducing individual selector device or making the memory self-selective. However, in 3D V-RRAM structure, introducing individual selector is not allowed, because the intermediate electrode could shorten the memory cell in the same column. Thus, the RRAM cell with self-selective characteristics is the only choice for 3D V-RRAM.

S3. Multi-level storage and retention of single HfO_2 layer device

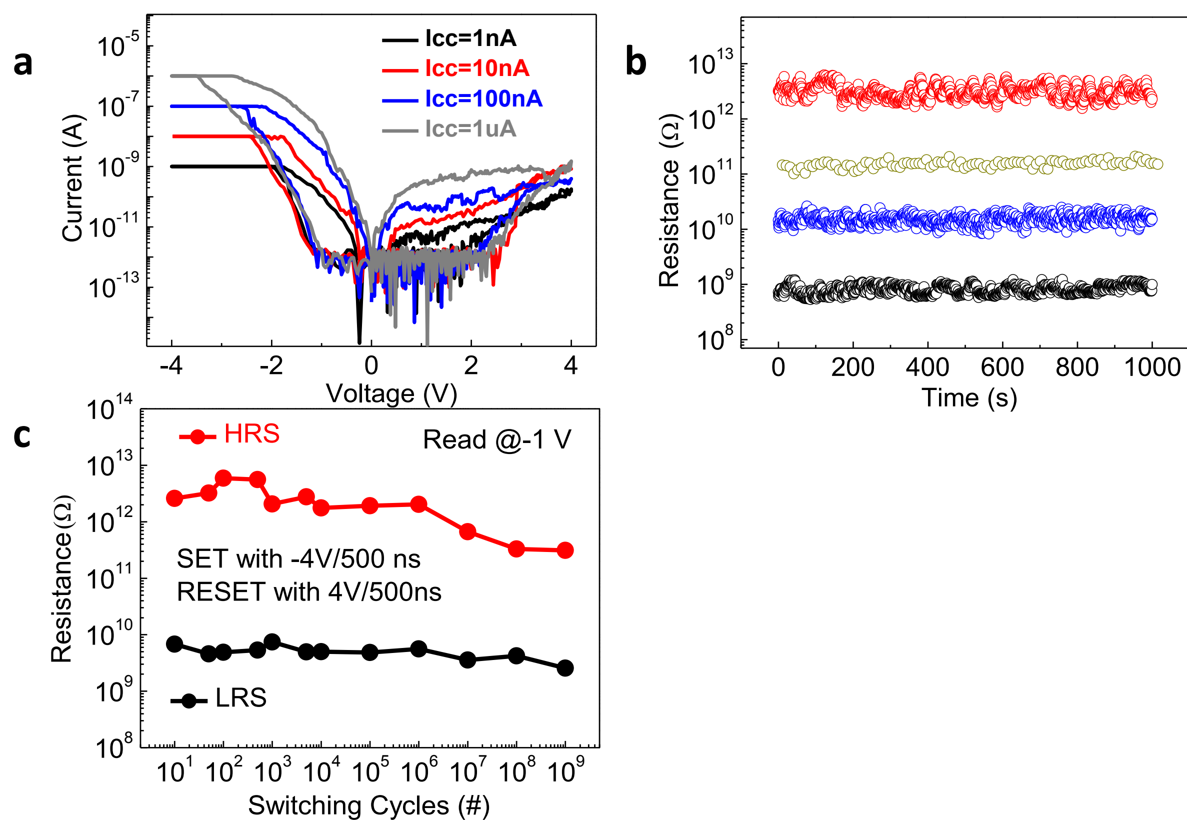

Fig. S3. a) Multi-level storage obtained by different compliance currents in single HfO_2 device; b) Retention of multi-level resistance states obtained by different compliance currents in single HfO_2 device; c) Endurance of single HfO_2 layer devices with ultra-low switching current. More than 10^9 cycles were achieved with sufficient sense margin.

S4. Conduction mechanism study of LRS

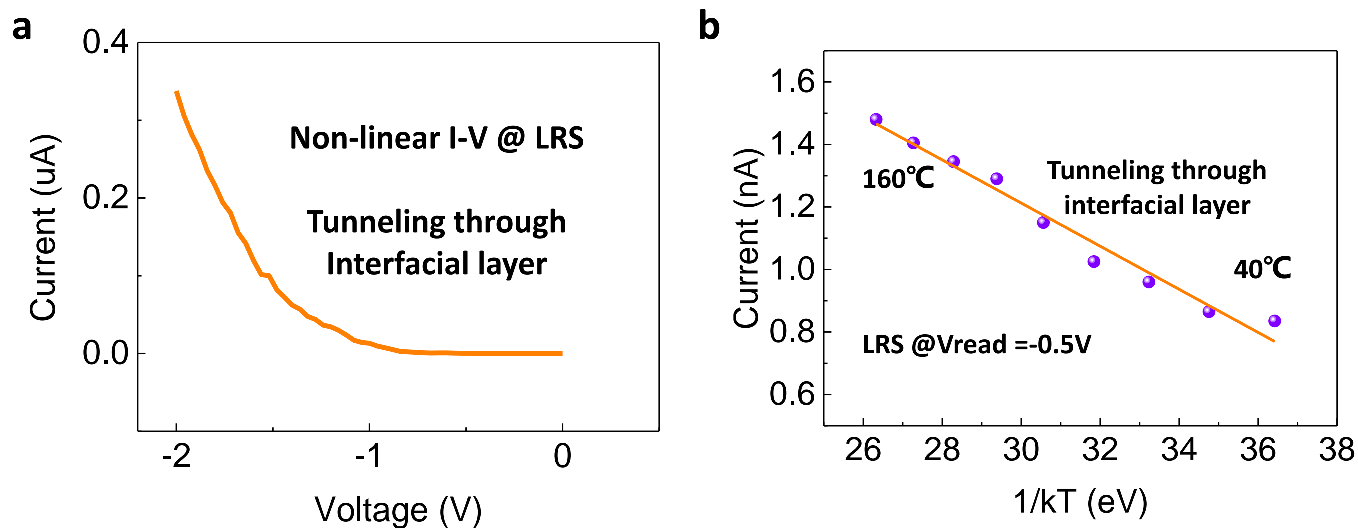

Fig. S4 (a)I-V curve in the LRS. (b) Temperature dependence of the LRS current. Non-linear I-V and a weak temperature dependence indicate that tunneling current through an interfacial layer is the dominate conduction mechanism in LRS. This result is analogous to the results reported by Shimeng Yu [43].

S5. Memory effect in the bilayer device

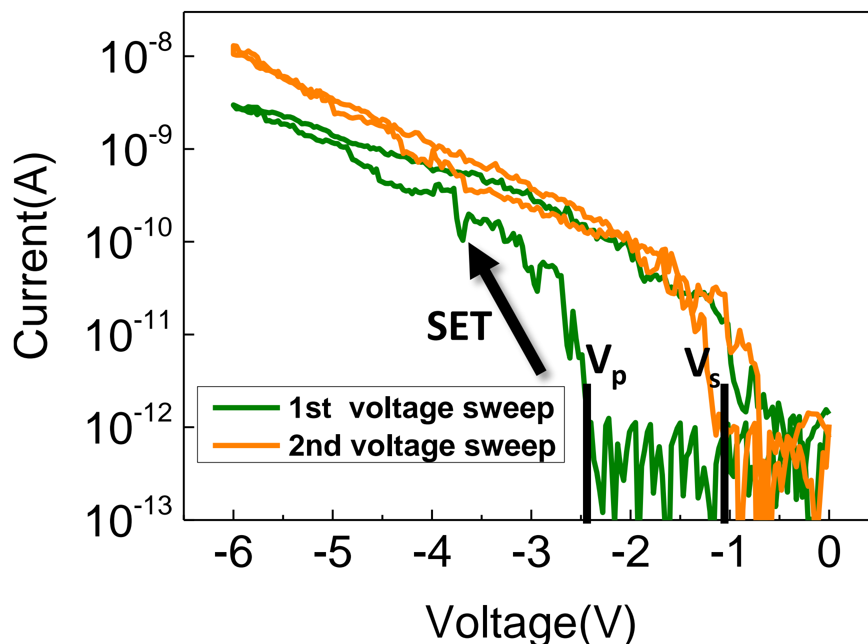

Fig. S5. I-V curves of successive voltage sweeping from 0→-6V→0. In the 1st sweeping loop, the resistive switching from off-state to on-state appears at V_p. The on-state resistance goes back to off-state at V_s during the backward sweeping (-6 V to 0). In the 2nd sweeping loop, the switching point of the device after previous programming is nearby V_s, rather than V_p. This is an evidence showing the bilayer device has memory effect. The switching voltage could be effectively tuned by programming.

S6 Schematic of proposed mechanism

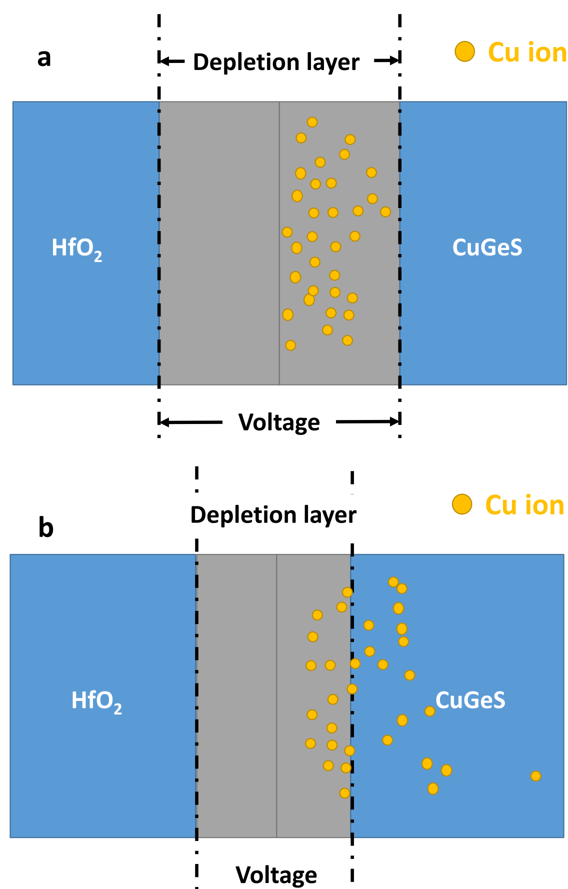

Fig. S6 a) Schematic of enhanced depletion layer. the Cu ions in the CuGeS layer are accumulated on the interface adjacent to the HfO_2 layer. An enhanced space charge depletion layer could be expected in the bilayer device.At low voltage, much of the voltage will apply on the enhanced depletion layer and the current remains low. b) Schematic of depletion layer after set operation. Under certain external voltage (e. g V_p), this depletion region could be narrowed by driving the Cu ions away from the interface, making the carriers conducting easier and thus increasing the device conductivity dramatically.

S7. The retention of bilayer BNR devices

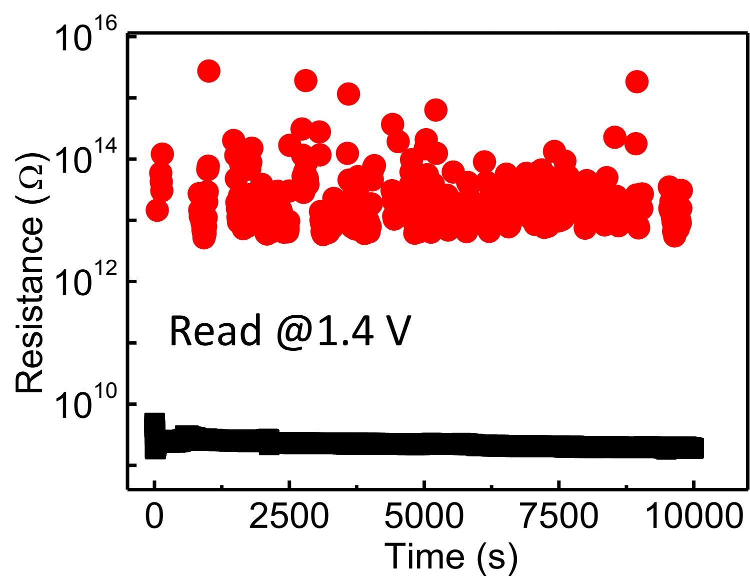

Fig. S7. Retention of bilayer self-selective cell with a reading voltage of 1.4 V. Both of HRS and LRS can be maintained for more than 10000s without obvious degradation.

S8. The high temperature retention of bilayer BNR devices

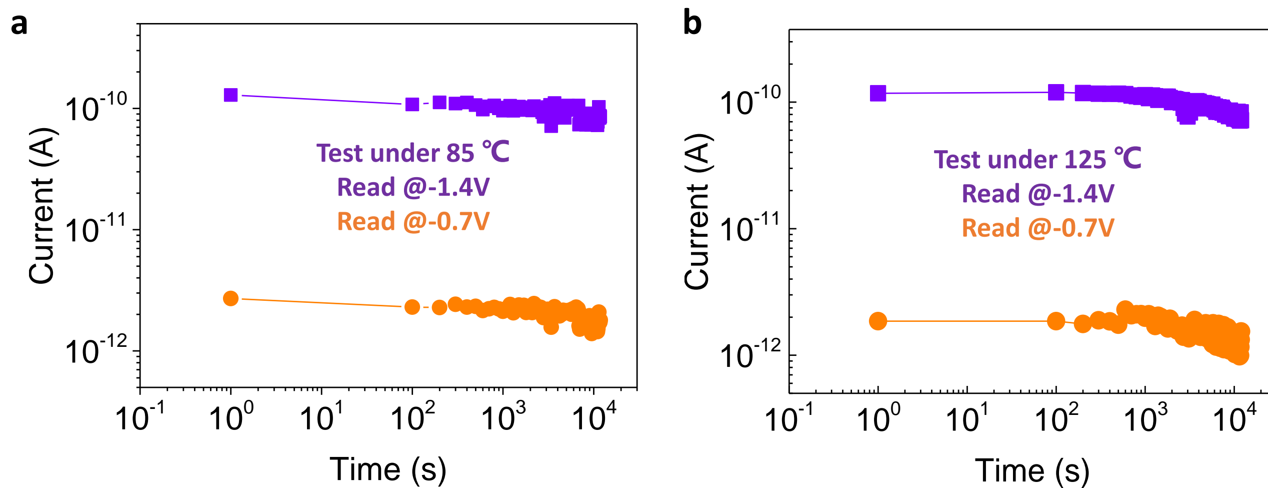

Fig. S8 Low resistance state retention test. The device can maintain its states for 10000s with a more than 100 times of nonlinearity.

S9. Read margin analysis in the worse-case scenario

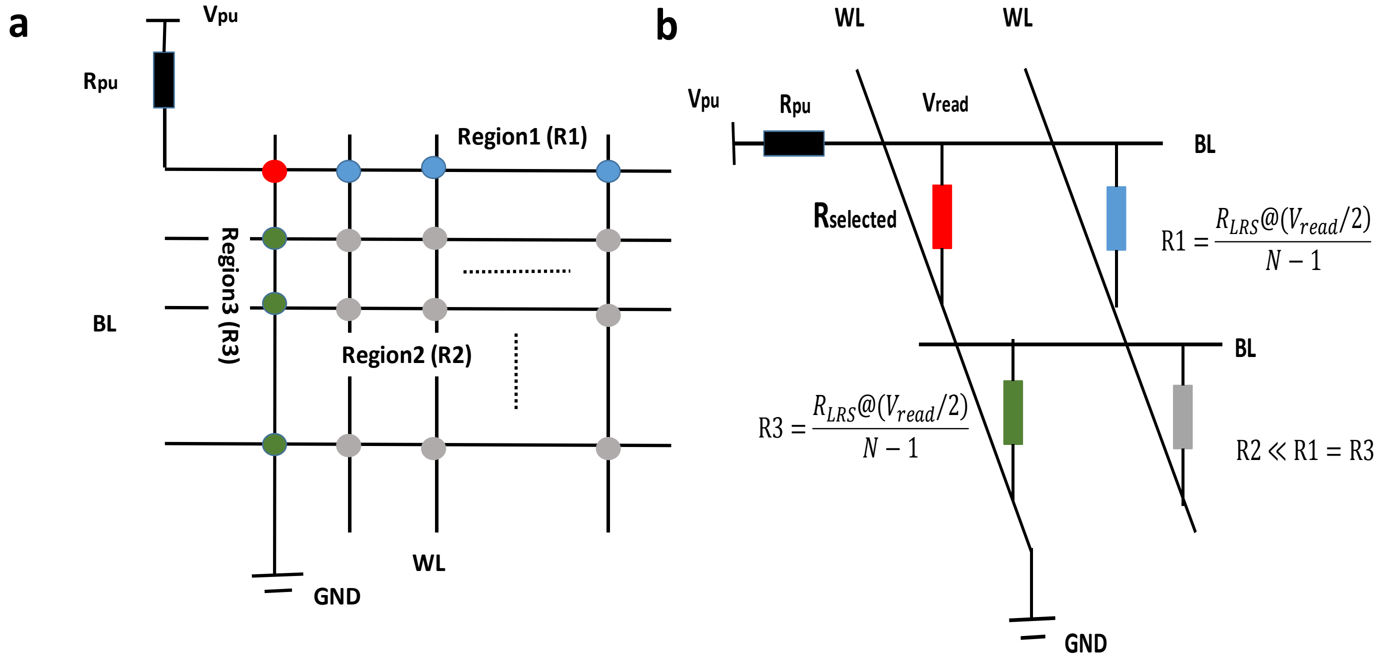

Fig. S9. a) Schematic of a square crossbar array. Unselected cells can be divided into three regions: R1, R2 and R3; b) The equivalent circuit in the worse-case scenario (only one BL pulled up and all unselected bits at LRS). V_{read} is dropped on the selected cell, while $V_{read}/2$ is dropped on the cells in the same row or column of selected cell. The quantitative assessment on the read margin $\triangle V$ normalized to the pull-up voltage V_{pu} can be calculated by solving the Kirchhoff equation:

$$\frac{\Delta V}{V_{pu}} = \frac{R_{pu}}{R_{LRS}(V_{read})\left\|\frac{2R_{LRS}(\frac{V_{read}}{2})}{N-1}+R_{pu}\right.} - \frac{R_{pu}}{R_{HRS}(V_{read})\left\|\frac{2R_{LRS}(\frac{V_{read}}{2})}{N-1}+R_{pu}\right.} \quad \text{(S1)}$$