Fully-integrated, Bezel-less Transistor Arrays Using Reversibly Foldable Interconnects and Stretchable Origami Substrates

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Experimental

Preparation of the foldable substrate: On the SiO_2 wafer, 800 nm-thick Cu was deposited using E-beam lithography (Woosung) as a sacrificial layer. SU-8 3050 (MicroChem Corp.) was spin-coated (2000 rpm, 30 sec) and patterned as rigid plates. Subsequently, PDMS (Dow Corning Co., Sylgard 184) mixing base with curing agent at 10:1 was also spin-coated (2000 rpm, 30 sec) and cured at 140 ˚C for 4 hrs. After that, the Cu sacrificial layer was selectively etched by diluted etching solution of $FeCl_3$: HCl: H_2O (1:1:20 vol.%).

Uniaxial tensile test: We performed uniaxial tensile testing of PDMS and PET. PDMS films of thickness 100 μm were prepared using same procedure as the foldable devices, and PET film of thickness 100 μm was chosen as a typical flexible substrate. Dog-bone-shaped tensile samples of 5 mm-gage length and 1 mm-width based on ASTM E638 were cut from two films. Uniaxial tensile testing using micro-universal testing machine (AGS-100N, Shimadzu Ltd., Japan) was carried out at a rate of 0.5 mm/min until sample rupture.

Finite element method simulations: We conducted FEM (finite element method) simulations of folding of PDMS and PET films using Abaqus 6.12; input files were created with Abaqus CAE. Stress-strain curves for the samples measured by uniaxial tensile testing were used as input material properties. A two-dimensional specimen of 0.1 mm-thickness and 10 mm-length was made up of 7002 3-node linear plane stress triangular elements (CPS3). Films were placed between rigid body walls and the walls were moved closer to induce the folding of the films. The friction coefficient between rigid wall and film was set to zero.

Formation of foldable hybrid film: For AgNWs on Au thin film, AgNWs ink from Nanopyxis Co., Ltd. (diameter: 100 nm, length: 50 μm) was spin-coated four times (500 rpm, 30 sec) on the Cu/SiO_2 wafer. Subsequently, 100 nm-thick Au was deposited by thermal evaporation. Then PDMS was spin-coated and cured at 140 ˚C for 4 hrs. The copper sacrificial layer was etched by diluted etching solution of $FeCl_3$: HCl: H_2O (1:1:20 vol.%). Au thin film on AgNWs was prepared by deposition of Au, spin-coating of AgNWs ink and formation of PDMS on the Cu/SiO_2 wafer.

Cyclic stretching test: Hybrid film was repeatedly stretched and released by a computer-controlled stretching stage with uniaxial 80% strain up to 10,000 cycles.

Fabrication of foldable TFT backplane: Lift-off resist (MicroChem Corp., LOR 3A) and positive photoresist (MicroChem Corp., s1805) were spin-coated and then used to pattern the electrodes on the Cu/SiO_2 wafer. Subsequently, a 3 nm-thick Cr / 100 nm-thick Au layer was deposited by thermal evaporation. It formed the gate line patterns after the remaining lift-off resist and photoresist were removed. For gate dielectric layer, 30 nm-thick Al_2O_3 is deposited on them by atomic layer deposition (LUCIDA D100, NCD), followed by etch-back process is progressed by using positive photoresist (s1805, MicroChem). An In_2O_3 solution was spin-coated and annealed at 250 ˚C for 2 hr 30 min on the hot plate. In_2O_3 with channel-patterned photoresist (s1805, MicroChem) was etched by Cr etchant; then a 3 nm-thick Cr / 100 nm-thick Au was patterned as data line and source/drain electrodes. For the foldable interconnects, spin-coated AgNWs (MicroChem Corp., s1818) with photoresist patterns along Au interconnects was dry-etched by oxygen reactive ion etching (RIE) plasma (O_2 60 sccm, 50 W, 240 sec) and wet-etched by Al etchant; successively, the foldable substrate was formed on them. The foldable TFT backplane was exfoliated from the handling substrate by etching the copper sacrificial layer.

Characterization and measurements: Optical measurements were taken by Cold FE-SEM (Hitachi) and optical microscope (BX53, OLYMPUS). Sheet resistance was measured by the four-probe method using a Keithley 4200-SCS semiconductor parametric analyzer. In addition, transfer characteristics (I_D-V_G), output characteristics (I_D-V_D), and resistance measurements were also conducted by the three-probe and two-probe method, respectively.

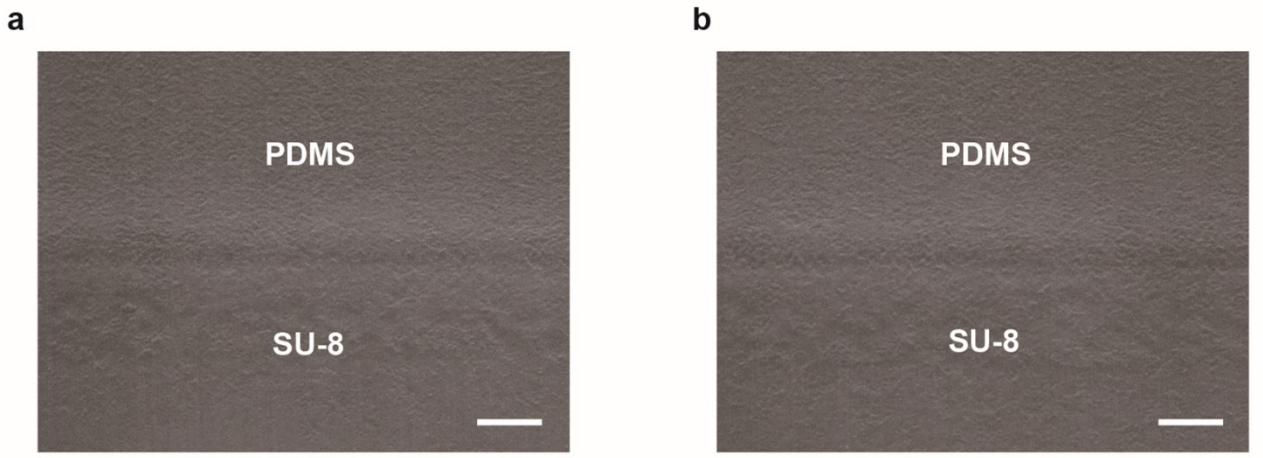


Fig. S1 Interface between PDMS and SU-8. (a) SEM image (top view) of rigid to soft transition zone before and (b) after 10,000 perfect folding cycles, respectively. PDMS and SU-8 adhere each other and form the smooth interface without the groove after folding cycles. Scale bar, 3 μm.

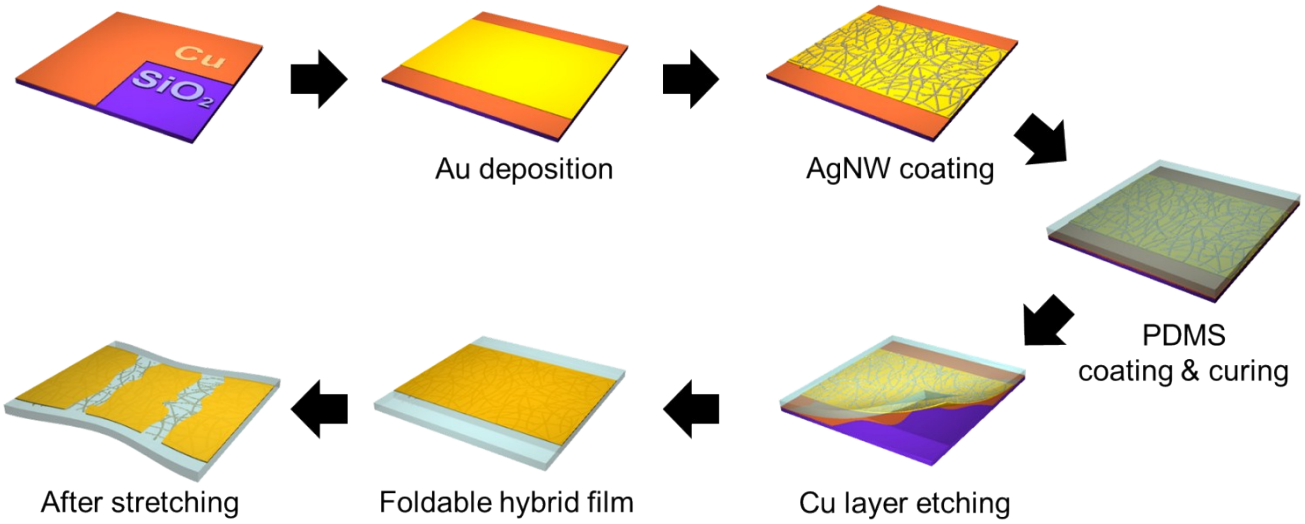


Fig. S2 Fabrication steps of foldable films (Au film on AgNWs).

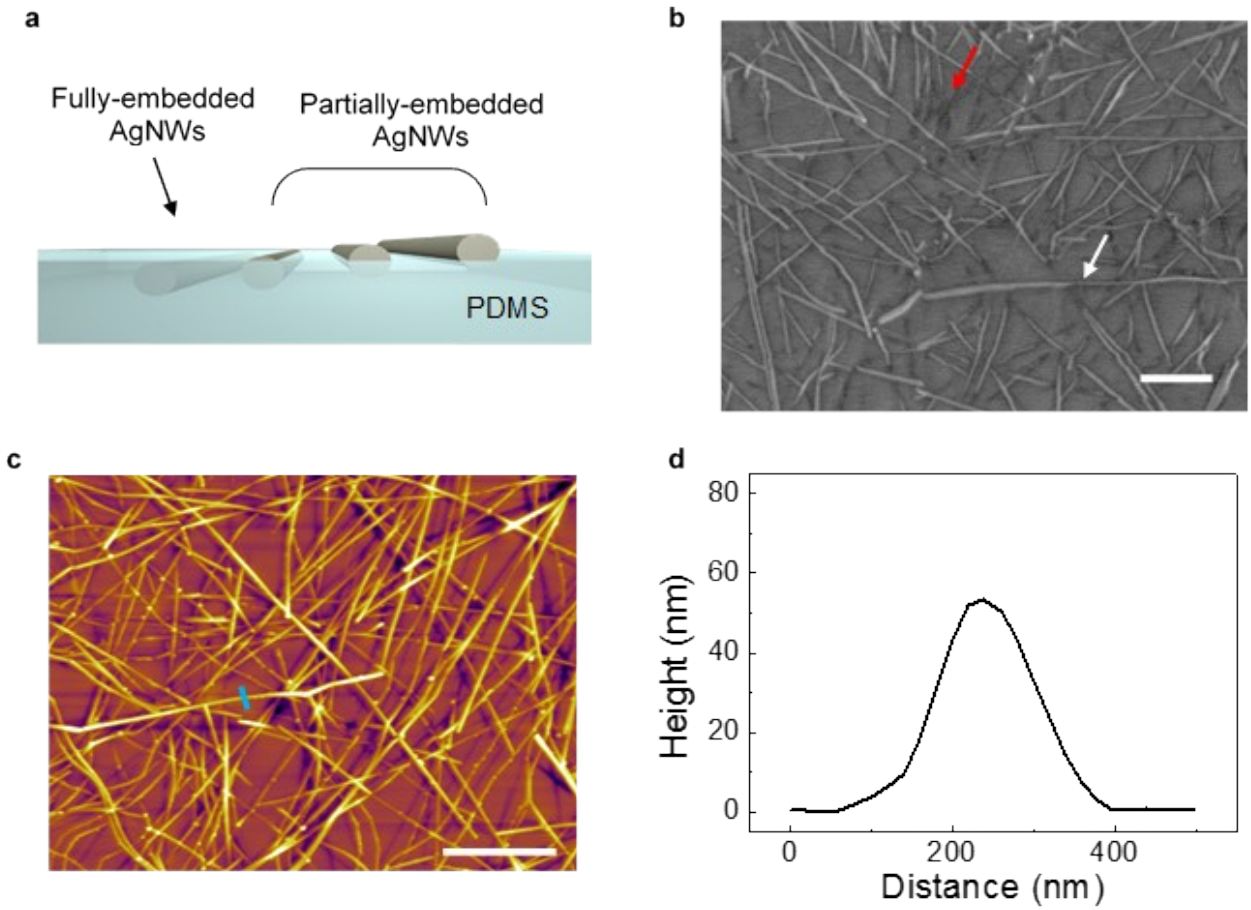


Fig. S3 Partially or near-fully embedded silver nanowires in PDMS. (a) Schematic image of fully or partially embedded AgNWs. (b) SEM image of partially (white arrow) or near-fully (red arrow) embedded AgNWs in PDMS. Scale bar, 2 μm. (c) AFM image of partially or near-fully embedded AgNWs. Therefore, AgNWs can endure the applied strain in spite of cracked gold. Scale bar, 5 μm. (d) Height profile of AFM image (blue line).

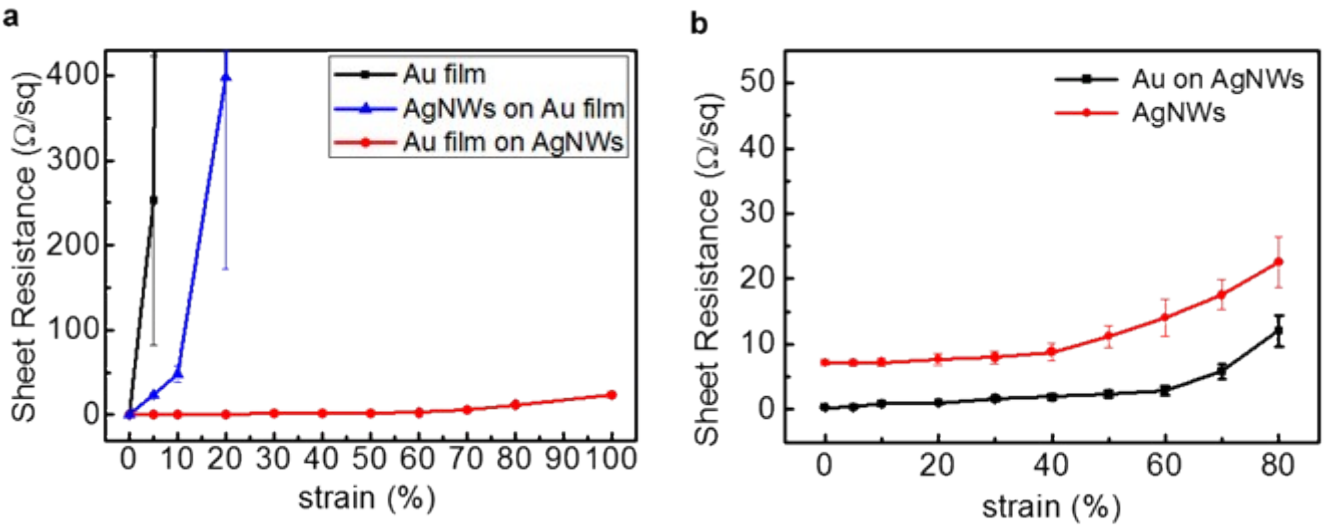


Fig. S4 Sheet resistance of hybrid foldable films as a function of tensile strain. (a) Sheet resistance of Au film (black line), AgNWs on Au film (blue line), and Au film on AgNWs (red line) as a function of tensile strain. This graph is the magnification of the graph in Fig. 3c. (b) Sheet resistance of Au on AgNWs (black line) and embedded AgNWs (red line) as a function of tensile strain. Because of high conductivity of gold thin film, AgNWs on Au shows lower sheet resistance compared to embedded AgNWs.

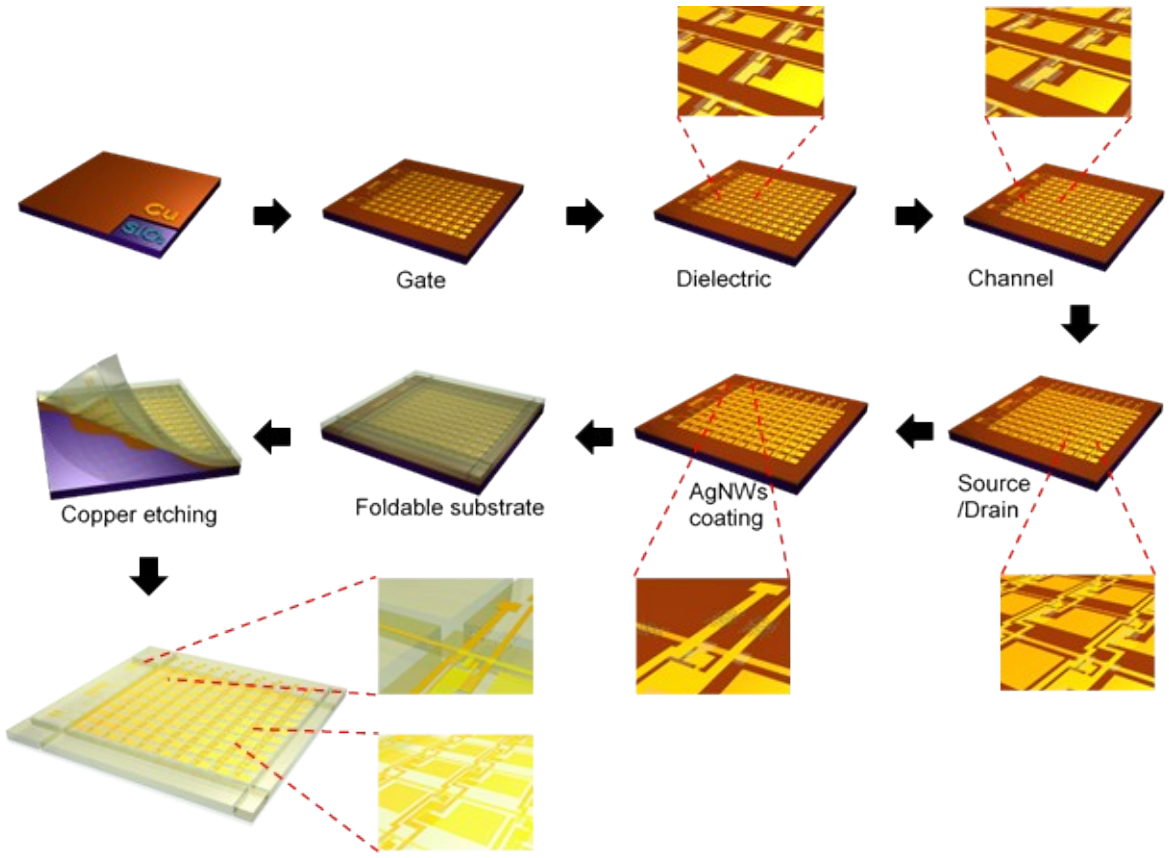


Fig. S5 Fabrication processing steps of foldable TFT backplane using transfer-free method. Using sacrificial layer, it is possible to fabricate the foldable TFT with high working temperature and high yield.

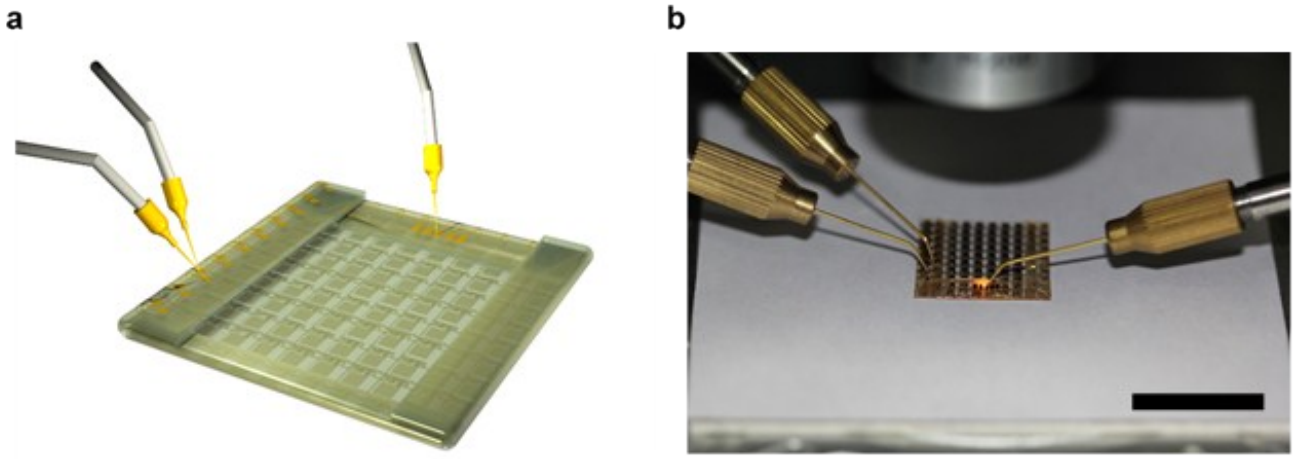


Fig. S6 Electrical measurement of bezel-less TFT arrays. (a) Schematic image of electrical measurment at the folded state. (b) Photograph of electrical measurement at the folded state. Scale bar, 2 cm.

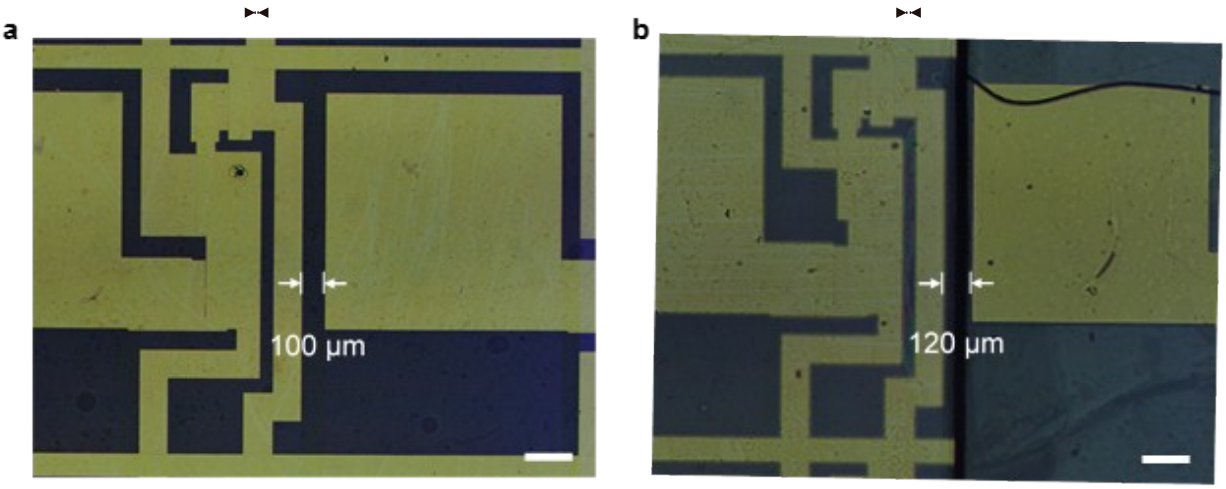
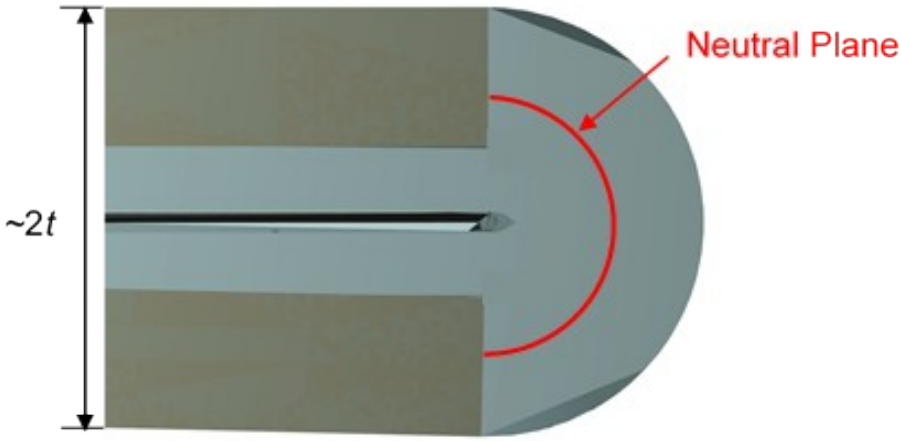


Fig. S7 Distance between transistors in zero-bezel TFT backplane. (a) Optical microscopic image of two transistors in one TFT backplane. The distance between the two transistors is ~100 μm. (b) Optical micrograph of two transistors which belong to each different TFT matrix. The distance between them is ~120 μm. Scale bars, 200 μm.

Movie S1. Reversible and perfect folding behavior of foldable substrates. This movie shows reversible folding process of electronic devices on the pre-designed foldable substrate. At that time, tensile strain was not applied to the devices.

Relation between thickness of foldable substrate (*t*) and gap width (*w*)



When substrate thickness is ***t***, thickness of perfectly folded substrate is ~2***t***. To reduce folding strain applied in PDMS, gap width should be designed using following equation:

$$\text{Gap width } (\boldsymbol{w}) \geq \text{Length of Neutral Plane}$$

In this case, Length of Neutral Plane $\approx 0.5 \times ((0.5 \times 2\boldsymbol{t}) \times \pi) = 0.5\ \pi\boldsymbol{t}$.

Therefore, we can obtain

$$\boldsymbol{w} \geq 0.5\ \pi\boldsymbol{t},$$

where ***t***: Substrate thickness, ***w***: Gap width

Thickness of our fabricated foldable substrate is 100 μm. By applying this equation, gap width should be greater than or equal to 50π μm. Therefore, we designed 200 μm of gap width of foldable substrate.

Calculation of resistance of foldable interconnects

Resistance can be easily calculated by following equation:

$$R = R_S \times \frac{L}{W},$$

where R: Resistance, R_S: Sheet resistance, L: Length of conductor, W: Width of conductor.

Maximum tensile strain applied in foldable conductor is about 80%. At 80% tensile strain, sheet resistance of foldable conductor shows ~12.1 Ω/sq.

In case of data lines, length and width of foldable interconnect at perfectly folded substrate are ~100π μm and 150 μm, respectively. And in case of gate line, length and width of foldable interconnect are ~200π μm and 150 μm, respectively. Therefore, we can calculate resistance of foldable interconnect of zero-bezel transistor.

- Resistance of foldable interconnects of data lines:

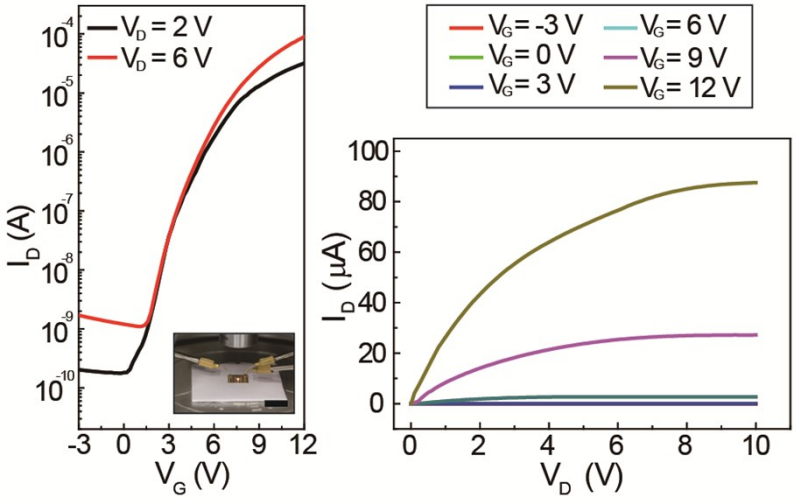
$12\ \Omega/\text{sq} \times \frac{100\pi}{150} \times 2$ (1 source line and 1 drain line) = ~50 Ω

- Resistance of foldable interconnects of gate line:

$12\ \Omega/\text{sq} \times \frac{200\pi}{150} \times 1$ (1 gate line) = ~50 Ω

Considering resistance of Cr/Au interconnects on rigid plates and foldable interconnects on elastomeric joints, the resistance of data and gate lines of a transistor in bezel-less TFT arrays is ~100 Ω

Calculation of On-resistance of transistors (R_{ON})



According to **Figure 4e** transfer and output characteristics of field-effect transistor (FET) on the foldable TFT backplane in the folded state, on-resistance of transistors can be calculated by following equation:

$$R_{ON} = \frac{V_D}{I_D(ON)},$$

where V_D : Drain voltage, $I_D(ON)$: Channel current in the on state, R_{ON}: On-resistance of transistor

- Linear region: at $V_D = 2$ V, $I_D(ON) = 3 \times 10^{-5}$ A and $R_{ON} = \frac{V_D}{I_D(ON)} = 6.7 \times 10^5\ \Omega$

- Saturation region: at $V_D = 6$V, $I_D(ON) = 9 \times 10^{-5}$ A and $R_{ON} = \frac{V_D}{I_D(ON)} = 6.7 \times 10^5\ \Omega$

Therefore, $R_{ON} \approx 6.7 \times 10^5\ \Omega$.