

Supporting information for

Black Phosphorus Nonvolatile Transistor Memory

Dain Lee,^{1†} Yongsuk Choi,^{1†} Euyheon Hwang,^{1,2} Moon Sung Kang,⁴ Seungwoo Lee,^{1,3} and Jeong Ho Cho^{1,3*}

¹SKKU Advanced Institute of Nanotechnology (SAINT), ²Department of Physics, ³School of Chemical Engineering, Sungkyunkwan University, Suwon 16419, Korea.

⁴Department of Chemical Engineering, Soongsil University, Seoul 156–743, Korea.

Corresponding author E-mail: jhcho94@skku.edu

[†]D. Lee and Y. Choi contributed equally this work.

Experimental section

Device fabrication: The nano floating gate transistor memories (NFGTMs) with few-layer black phosphorus (BP) were fabricated onto a heavily-doped Si wafer with a 300 nm-thick SiO₂ layer, where Si was utilized as the gate electrode, while SiO₂ was utilized as the blocking gate dielectric layer. The SiO₂ surface was cleaned by UV/ozone treatment (254 nm, 28 mW/cm²) for 15 minutes. The AuNPs with a diameter of around 9 nm were deposited by thermal evaporation method onto SiO₂ substrate at a rate of 0.01 nm/s. The propylene glycol monomethyl ether acetate (PGMEA) solution composed of 1 wt% poly-4-vinylphenol (PVP, $M_w = 20,000$ g mol⁻¹) and 0.5 wt% poly(melamine-co-formaldehyde) (PMF, $M_w = 511$ g mol⁻¹) was spin-coated onto the AuNPs/SiO₂/Si substrate. The resulting film was thermally annealed in vacuum oven at 180 °C for 2 hrs to generate cross-linking of PVP. Few-layer BP flakes were exfoliated mechanically from bulk BP crystals using a Scotch adhesive tape and then transferred onto the cross-linked PVP (cPVP) surface in an Ar glove box to prevent degradation induced by the exposure of the material to water or oxygen during the fabrication processes. The source/drain electrodes (Ni/Au thickness = 20/40 nm) were defined through conventional e-beam lithography processes. Finally, the devices were passivated by spin-coating of 200 nm thick-PMMA ($M_w = 200,000$) and subsequent baking at 200 °C for 15 minutes.

Measurements: The surface morphology of the mechanically-exfoliated BP flake was obtained by a tapping-mode atomic force microscopy (AFM, D3100 Nanoscope V, Veeco). Raman spectrum was measured by a confocal Raman microscope (Alpha 300R, Witec). The electrical properties of the BP-NFGTMs were measured using Keithley 2400 and 236 source/measure units at room temperature in the dark under vacuum ($\sim 10^{-4}$ Torr).

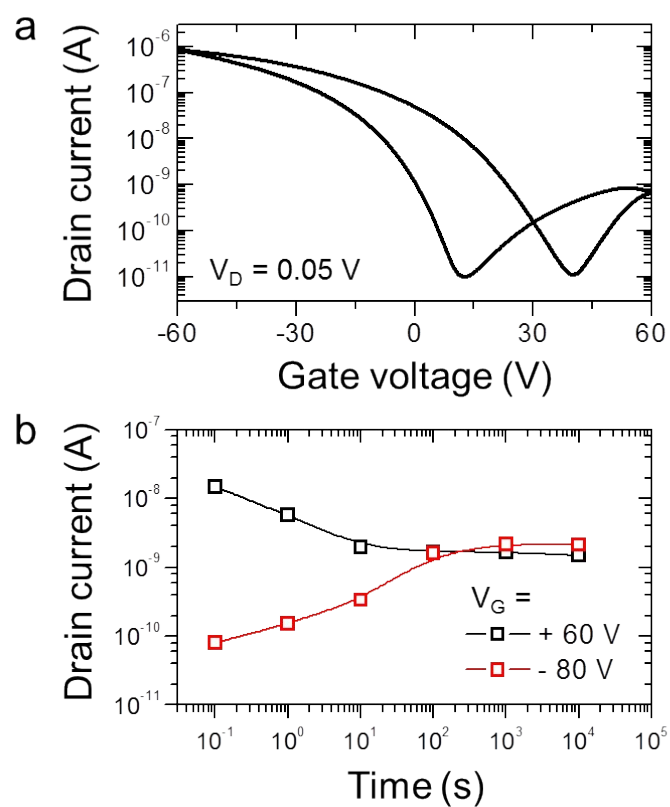


Figure S1. (a) Transfer characteristics and (b) Retention time characteristics of the BP transistors without AuNPs.