

SUPPORTING INFORMATION

**Lithography-free plasma-induced patterned growth of MoS₂ and its
heterojunction with graphene**

Xiang Chen, Yong Ju Park, Tanmoy Das, Houk Jang, Jaebok Lee and Jong-Hyun Ahn[†]

School of Electrical and Electronic Engineering, Yonsei University, 50 Yonsei-ro,
Seodaemun-gu, Seoul 03722, Republic of Korea.

[†]E-mail: ahnj@yonsei.ac.kr

Contents:

Supplementary Figure S1-S4

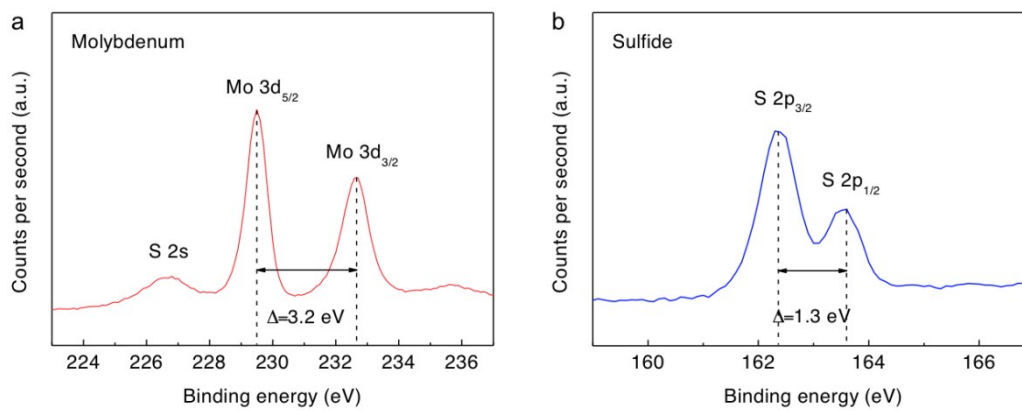


Fig. S1 (a, b) X-ray photoemission spectroscopy (XPS) results of the binding energy for Molybdenum (a) and Sulfide (b) from patterned monolayer MoS₂.

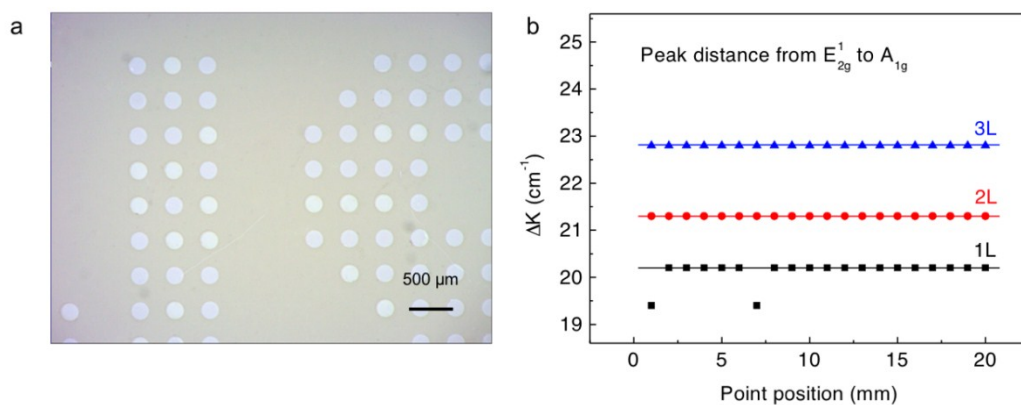


Fig. S2 (a) Optical microscope image of a part of “YONSEI” mark consists of patterned MoS₂ layers in circle shape after transferred onto sapphire substrate. (b) Peak distances of E_{2g}¹ and A_{1g} peaks for 20 measurement points from the patterned 1L-3L MoS₂ on SiO₂ substrate in size of 2 × 2 cm.

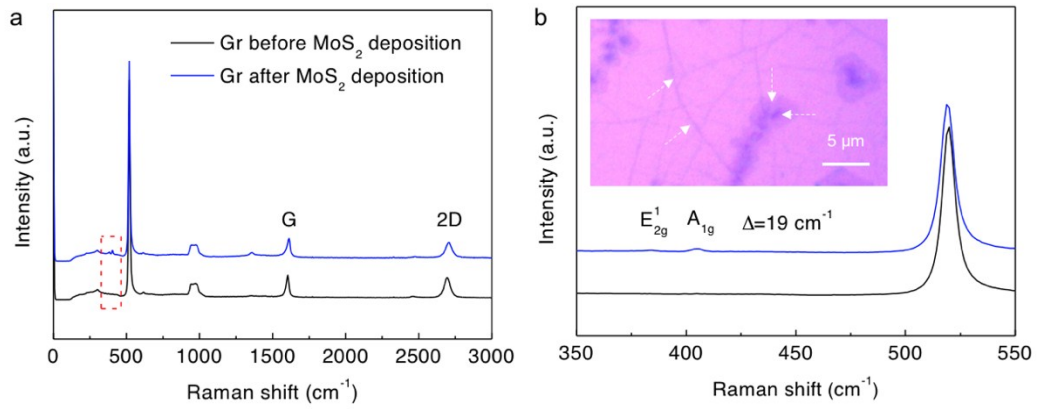


Fig. S3 (a, b) Raman spectra of bilayer CVD graphene before and after MoS_2 deposition in large (a) and small (b) ranges. Inset shows the optical microscope image of bilayer graphene after MoS_2 growth, and MoS_2 tends to grow along the wrinkles or on the 2L/3L graphene seeds.

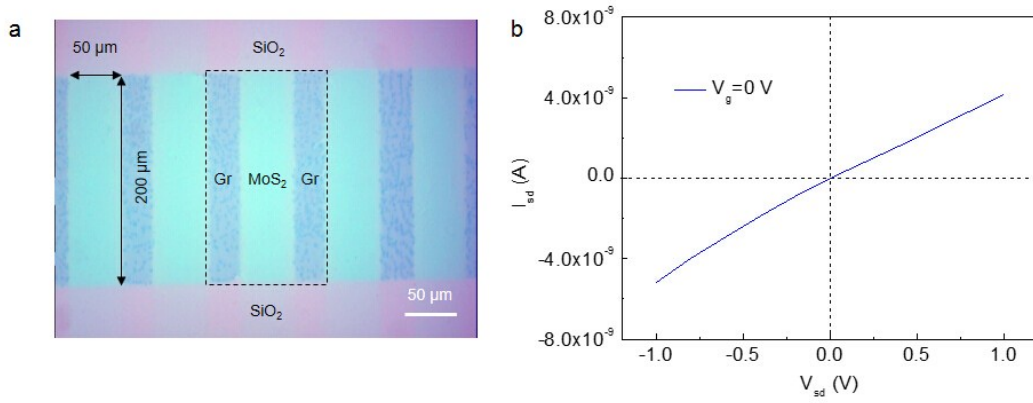


Fig. S4 (a) Optical microscope image of a transistor unit composed of MoS₂ channel and graphene electrodes, as marked in the black box. The length and width of the MoS₂ channel are 50 μm and 200 μm, respectively. The top and bottom parts have been etched by using CHF₃/O₂ plasma (35/10 sccm, 100 W, 6 s) with help of a shadow mask. (b) I-V electrical property of the transistor. The source-drain bias (V_{sd}) was swept from -1 V to 1 V, and the back-gate voltage (V_g) was 0 V.